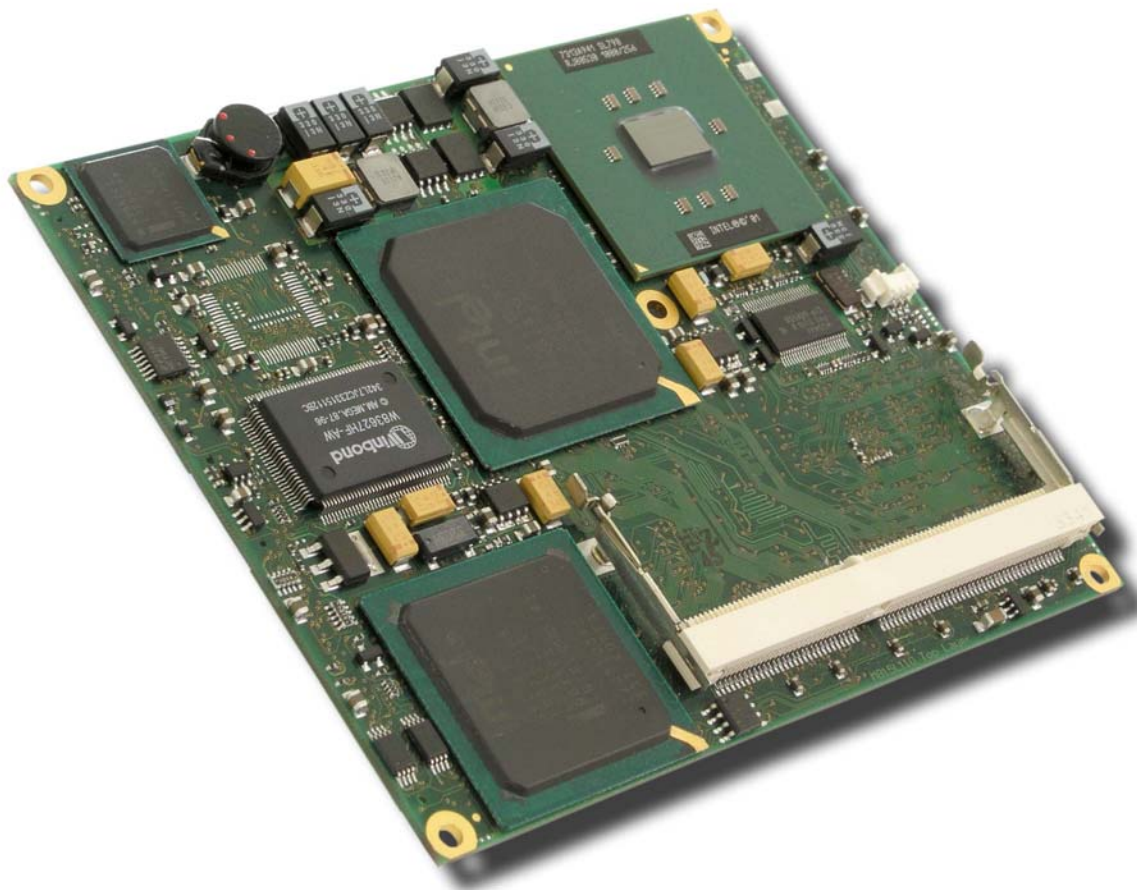


► Kontron User's Guide



► ETX®-P3T

Document Revision 1.15

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1 User Information

1.1 About This Document

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1.4 Standards

Kontron Embedded Modules GmbH is certified to ISO 9000 standards.

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1.6 Technical Support

Technicians and engineers from Kontron Embedded Modules GmbH and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Before contacting Kontron Embedded Modules GmbH technical support, please consult our Web site at <http://www.kontron-emea.com/emd> for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone or email.

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2 Introduction

2.1 ETX®-P3T

ETX®-P3T component SBC modules support the Intel® Celeron® processor. The ETX®-P3T features an Intel® 815 chipset graphics memory controller hub.

In addition to standard ETX® features, the *ETX®-P3T* supports four 2.0 USB ports, 10/100Base-T Ethernet, keyboard/mouse controllers, a real-time clock, and a watchdog timer.

2.2 ETX® Documentation

This product manual serves as one of three principal references for an ETX® design. It documents the specifications and features of *ETX®-P3T*. The other two references, which are available from the Kontron Embedded Modules Web site, include:

- The ETX® Component SBC™ Specification defines the ETX® module form factor, pinout, and signals. You should read this first.
- The ETX® Component SBC™ Design Guide serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a range of ETX® modules.

2.3 ETX® Benefits

Embedded technology extended (ETX®) modules are very compact (~100mm square, 12mm thick), highly integrated computers. All ETX® modules feature a standardized form factor and a standardized connector layout that carry a specified set of signals. This standardization allows designers to create a single-system baseboard that can accept present and future ETX® modules.

ETX® modules include common personal computer (PC) peripheral functions such as:

- Graphics
- Parallel, Serial, and USB ports
- Keyboard/mouse
- Ethernet
- Sound
- IDE

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

Peripheral PCI or ISA buses can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard using the computer as one plug-in component simplifies packaging, eliminates cabling, and significantly reduces system-level cost.

A single baseboard design can use a range of ETX® modules. This flexibility can differentiate products at various price/performance points, or to design future proof systems that have a built-in upgrade path. The modularity of an ETX® solution also ensures against obsolescence as computer technology evolves. A properly designed ETX® baseboard can work with several successive generations of ETX® modules.

An ETX® baseboard design has many advantages of a custom, computer-board design but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

3 Specifications

3.1 Functional Specifications

Processor

- *ETX@-P3T*: Intel® Celeron® Processor (0.13 μ) in Micro-FCBGA (μBGA479) 400MHz and 733MHz Ultra Low Voltage and 1GHz Low Voltage.

Bus

- 100MHz (Celeron® 400MHz)/133MHz (Celeron® 733MHz and 1000MHz) CPU bus
- 100MHz (Celeron® 400MHz)/133MHz (Celeron® 733MHz and 1000MHz) memory bus

Chipset: Intel® 815

Super I/O: Winbond W83627HF connected by using an LPC interface

Cache: On-die Second level 256k

Memory

- One 144-pin SO-DIMM
- 3.3V PC-PC-133 or PC-100 unbuffered SDRAM, up to 512MB (512MB 16 chip modules only)

Two Serial Ports (COM1 and COM2)

- Transistor-to-transistor (TTL) signals only
- Standard RS232C
- 16550 compatible

Infrared Device Association (IrDA) interface

One Parallel Port (LPT1)

- Shared with Floppy signals
- Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP) with bi-directional capability

Floppy: Shared with LPT signals

Enhanced Intelligent Drive Electronics (EIDE): Two Peripheral Component Interconnect (PCI) Bus Master IDE ports (up to four devices) support:

- Ultra 100/66/33 Direct Memory Access (DMA) mode
- Programmed Input/Output (PIO) modes up to Mode 4 timing

- Multiword DMA Mode with independent timing

Universal Serial Bus (USB)

- Four USB 1.1/2.0 ports (UHCI and EHCI)
- USB legacy keyboard support
- USB floppy, CD-ROM, Hard drive, and memory stick boot support

Integrated Ethernet: Intel 82562 10/100 Mbps Fast Ethernet controller

- Integrated, WfM 2.0 and IEEE 802.3 compliant; 10BASE-T and 100BASE-TX compatible PHY

Onboard video graphics array (VGA): Integrated in Intel® 815:

- Graphics memory controller hub
- Up to 1MB Video RAM (UMA)
- Cathode ray tube (CRT) and low voltage differential signaling (LVDS) liquid-crystal display (LCD) interfaces.

Audio: Integrated in Intel 82801DB southbridge

- SoundBlaster™ AC97, Windows Sound System™ compatible

BIOS: Phoenix, 512k Flash-BIOS

- NV-EEPROM for CMOS-setup retention without battery

PS/2 keyboard controller

PS/2 mouse interface

Watchdog timer (WDT) integrated in the Super I/O (Winbond 83627HF)

Real-time clock (requires external battery)

BIOS support for additional super I/O devices (COM3, COM4, LPT, and Floppy)

3.2 Mechanical Specifications

3.2.1 Dimensions

- 95.0 mm x 114.0 mm (3.75" x 4.5")
- Height approx. 12 mm (0.4")

3.3 Electrical Specifications

3.3.1 Supply Voltage

- 5V DC +/- 5%

3.3.2 Supply Voltage Ripple

- Maximum 100 mV peak to peak 0 – 20 MHz

3.3.3 Supply Current 5 V_{SB}

- Typical 200 mA, peak 250 mA

3.3.4 Supply Current (typical, DOS prompt)

Power-consumption tests were executed during the DOS prompt and without a keyboard. Using a keyboard takes an additional 100 mA.

All tested boards were fully equipped –AL boards. All boards were equipped with 64MB SDRAM.

ETX®-P3T Celeron 400MHz

CPU Clock	Celeron 400 MHz		
Revisions	Layout 112 Bios Rev. 112		
Mode	Full On	Standby	Suspend
Power Consumption	2.2 A	1.8 A	1.8 A

ETX®-P3T Celeron 733MHz

CPU Clock	Celeron 733 MHz		
Revisions	Layout 114 Bios Rev. 112		
Mode	Full On	Standby	Suspend
Power Consumption	2.9 A	2.0 A	2.0 A

ETX®-P3T Celeron 1000MHz

CPU Clock	Celeron 1000 MHz		
Revisions	Layout 112 Bios Rev. 112		
Mode	Full On	Standby	Suspend
Power Consumption	3.2 A	2.0 A	2.0 A

CMOS Battery Power Consumption

RTC	Voltage Range	Quiescent Current
Integrated in the southbridge	2.0 V - 3.6 V	3.77 µA @ 3.0 V

CMOS battery power consumption was measured with an ETX®-P3T module on a standard Kontron ETX® evaluation board. The system was turned off and the battery was removed from the evaluation board.

The 3.0 V of power was supplied from a DC power supply. Do not rely only on the above measured values to calculate the CMOS battery lifetime. We recommend that you measure the current using a complete application in a worst case scenario setting (high temperature/ high battery voltage). When calculating CMOS battery lifetime you must also consider the self-discharge of the battery. For detailed information see the INTEL 82801DB and Winbond W83627HF datasheets.

3.4 Environmental Specifications

3.4.1 Temperature

Operating: (with Kontron Embedded Modules heat-spreader plate assembly):

- Ambient temperature: 0 to +60 °C
- Maximum heatspreader-plate temperature: 0 to +60 °C (*)

Non-operating: -40 to +85 °C

See the [Thermal Management](#) chapter for additional information.

*Note: *The maximum operating temperature with the heatspreader plate is the maximum measurable temperature on any spot on the heatspreader's surface. You must maintain the temperature according to the above specification.*

Operating (without Kontron Embedded Modules heat-spreader plate assembly):

- Maximum operating temperature: 0 to +60 °C (**)

Non operating: -40 to +85 °C

See the [Thermal Management](#) chapter for additional information.

*Note: **The maximum operating temperature is the maximum measurable temperature on any spot on a module's surface. You must maintain the temperature according to the above specification.*

3.4.2 Humidity

Operating: 10% to 90% (non condensing)

Non operating: 5% to 95% (non condensing)

3.5 MTBF

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50° C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40° C in an office or telecommunications

environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

System MTBF (hours) : 147.789

Notes: *Fans usually shipped with Kontron Embedded Modules GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement. Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered for separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power; the only battery drain is from leakage paths.*

4 CPU, Chipset, and Super I/O

4.1 CPU

The central processing unit (CPU) consists of Mobile Intel® Celeron®, which includes such features as:

- Supports the Intel Architecture with Dynamic Execution
- On-die primary 16-Kbyte instruction cache and 16-Kbyte write-back data cache
- On-die second level cache (256-Kbyte) with Advanced Transfer Cache Architecture
- Data Prefetch Logic
- Integrated math co-processor
- Support for MMX™ technology
- Support for Streaming SIMD Extensions
- Power Management Features Quick Start, Deep Sleep and Deeper Sleep modes provide low power dissipation

4.2 Chipset

The chipset consists of:

- Intel® 815 (north bridge)
- Intel® 82801DB (south bridge)

4.3 Super I/O

- The super I/O device is a Winbond 83627HF

5 System Memory

The *ETX®-P3T* uses 144-pin Small Outline-Dual Inline Memory Modules (SO-DIMMs). One socket is available for a 3.3-volt, unbuffered PC-133 or PC-100 SDRAM module of either 32, 64, 128, 256, or 512MB (512MB 16 chip modules only) capacity.

6 Connector X1 Subsystems

6.1 PCI Bus

The implementation of this subsystem complies with the *ETX® Specification*. Implementation information is provided in the *ETX® Design Guide*. Refer to the documentation for additional information.

6.2 USB

Three USB host controllers (two 1.1 UHCI and one EHCI high-speed 2.0 controller) are on the Intel® 82801DB south bridge device. The USB controllers comply with both version 1.0 and 2.0 of the USB standard and are backward compatible. The three controllers implement a root hub, which have two USB ports each.

Configuration

The USB controllers are PCI bus devices. The BIOS allocates required system resources during configuration of the PCI bus.

6.3 Audio

The *ETX®-P3T* PCI audio controller is integrated in the Intel® 82801DB southbridge. The audio codec is compatible with AC97 and SoundBlaster Pro™.

Configuration

The audio controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI device.

6.4 Serial IRQ

The serial IRQ pin offers a standardized interface to link interrupt request lines to a single wire.

Configuration

The serial IRQ machine is in “Quiet Mode”, the frame size is 21 frames and the frame pulse width is 4 clocks.

6.5 3.3V Power Supply for External Components

The *ETX®-P3T* offers the ability to connect external 3.3V devices to the onboard-generated supply voltage. Pin 12 and Pin 16 of Connector X1 are used to connect to the +3.3V $\pm 5\%$ power supply. The maximum external load is 500mA. Contact Kontron Embedded Systems Technical Support for help with this feature.

Warning: Do not connect 3.3V pins to an external 3.3V supply.

For additional information, refer to the *ETX® Design Guide*, I²C application notes, and JIDA specifications, all of which are available on the Kontron Embedded Systems Web site.

7 Connector X2 Subsystems

7.1 ISA Bus Slot

The implementation of this subsystem complies with the *ETX® Specification*. Implementation information is provided in the *ETX® Design Guide*. Refer to the documentation for additional information.

8 Connector X3 Subsystems

8.1 VGA Output

The *ETX®-P3T* graphics subsystem is integrated in the Intel® 815 northbridge. It has the following features:

- 3D Hyper Pipelined Architecture
- Full 2D H/W Acceleration
- Motion Video Acceleration
- Mip Maps with Trilinear and Anisotropic Filtering
- Integrated 24-bit 230 MHz RAMDAC
- Gamma Corrected Video
- DDC2B Compliant
- Up to 1600x1200 in 8-bit Color at 85 Hz Refresh
- Hardware Accelerated Functions
- 3 Operand Raster BitBLTs
- 64x64x3 Color Transparent Cursor
- It can drive cathode ray tube (CRT) monitors and flat-panel displays, using the JUMPtect Intelligent LVDS Interface (JILI). You can program the graphics controller to use up the 1MB of unified memory architecture (UMA) memory as its video memory.
- Max. resolution CRT
- 1280x1024 @ 85 Hz 24bit
- 1600x1200 @ 75 Hz 8bit
- Max. resolution LCD
- SXGA 1400x1050 (4G colors)
- Bits/Pixels supported 1x18, 2x18, 1x24, and 2x24

Configuration

The graphics controller requires the following resources:

- An IRQ
- Several I/O addresses
- Memory-address blocks in high memory

The BIOS allocates the resources during AGP configuration. Many resources are set for compatibility with industry-standard settings.

8.2 LVDS Flat Panel Interface (JILI)

The user interface for flat panels is the JUMPtEC Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the *ETX® Specification*. Implementation information is provided in the *ETX® Design Guide*. Refer to the documentation for additional information.

8.3 Serial Ports (1 and 2)

The *ETX®-P3T* supports two serial interfaces (TTL). You can use COM2 for IrDA SIR operation. This feature is implemented in the super I/O device, which is a Winbond 83627HF.

The implementation of the serial interface complies with the *ETX® Specification*. Implementation information is provided in the *ETX® Design Guide*. Refer to the documentation for additional information.

Configuration

The serial-communication interface uses I/O and IRQ resources. The resources are allocated by the BIOS during POST configuration and are set to be compatible with common PC/AT settings. Use the BIOS setup to change some parameters that relate to the serial-communication interface.

8.4 PS/2 Keyboard

The implementation of the keyboard interface complies with the *ETX® Specification*. Implementation information is provided in the *ETX® Design Guide*. Refer to the documentation for additional information.

Configuration

The keyboard uses I/O and IRQ resources. The BIOS allocates the resources during POST configuration. The resources are set to be compatible with common PC/AT settings. Use the BIOS setup to change some keyboard-related parameters.

8.5 PS/2 Mouse

The implementation of the mouse interface complies with the *ETX® Specification*. Implementation information is provided in the *ETX® Design Guide*. Refer to the documentation for additional information.

Configuration

The mouse uses I/O and IRQ resources. The BIOS allocates the resources during POST configuration. The resources are set to be compatible with common PC/AT settings. You can change some mouse-related parameters from the BIOS setup.

8.6 IrDA

The *ETX®-P3T* is capable of IrDA SIR operation. This feature is implemented in the Winbond 83627HF. Contact Kontron Embedded Systems for help with this feature.

8.7 Parallel Port

The parallel-communication interface shares signals with the floppy-disk interface. The implementation of this parallel port complies with the *ETX® Specification*. Implementation information is provided in the *ETX® Design Guide*. Refer to the documentation for additional information.

Configuration

The parallel-communication interface uses I/O, IRQ, and DMA resources. The resources are allocated by the BIOS during POST configuration and are set to be compatible with common PC/AT settings. You can change some parameters of the parallel-communication interface through the BIOS setup.

8.8 Floppy

The floppy-disk interface shares signals with the parallel-communication interface. The floppy interface is limited to one drive (drive_1). A standard floppy cable has two connectors for floppy drives. One connector has a non-twisted cable leading to it, the other has a twisted cable leading to it. When using the floppy interface you must connect the floppy drive to the connector (drive_1) that has the non-twisted cable leading to it.

The implementation of this subsystem complies with the *ETX® Specification*. Implementation information is provided in the *ETX® Design Guide*. Refer to the documentation for additional information.

Configuration

The floppy-disk controller uses I/O, IRQ, and direct memory access (DMA) resources. These resources are allocated by BIOS during POST configuration and are compatible with common PC/AT settings. You can change some parameters of the parallel-communication interface through the BIOS setup.

9 Connector X4 Subsystems

9.1 IDE Ports

The IDE host adapter is capable of DMA-100/66/33 operation. The implementation of this subsystem complies with the *ETX® Specification*. Implementation information is provided in the *ETX® Design Guide*. Refer to those documents for additional information.

Note: **For UDMA-100/66 operation please follow the System Guidelines for ULTRA DMA of the ATA-Specification. The ETX®-concept in combination with peripheral devices (cable, connectors, base board layout...) can worse the transmission quality so that it is necessarily to decrease the UDMA-Mode to values below 3.*

Configuration

Primary and secondary IDE host adapters are PCI bus devices. They are configured by the BIOS during PCI device configuration. You can disable them in setup. Resources used by the primary and secondary IDE host adapters are compatible with the PC/AT.

Note: *PHOENIX BIOS will not recognize a Slave device on an IDE port if there is no Master device connected to the same IDE port.*

9.2 Ethernet

The Ethernet interface is based on the Intel® 82562 Fast Ethernet PCI controller. This 32-bit PCI controller is a fully integrated 10/100BASE-TX LAN solution.

The Ethernet interface requires an external transformer. See the *ETX® Design Guide* for suggestions on transformer selection.

Configuration

The Ethernet interface is a PCI device. The BIOS setup automatically configures it during configuration of the PCI device.

Note: *Implementation and limitation information is provided in the ETX® Design Guide from document revision 2.1. Refer to the documentation for additional information.*

9.3 Power Control

9.3.1 Power Good / Reset Input

The *ETX®-P3T* provides an external input for a power-good signal or a manual- reset pushbutton. The implementation of this subsystem complies with the *ETX® Specification*. Implementation information is provided in the *ETX® Design Guide*. Refer to the documentation for additional information.

9.4 Power Management

9.4.1 ATX PS Control

The *ETX®-P3T* can control the main power output of an ATX-style power supply. The implementation of this subsystem complies with the *ETX® Specification*. Implementation information is provided in the *ETX® Design Guide*. Refer to the documentation for additional information.

9.4.2 External SMI Interrupt

Contact Kontron Embedded Modules technical support for information on this feature.

9.5 Miscellaneous Circuits

9.5.1 Speaker

The implementation of the speaker output complies with the *ETX® Specification*. Implementation information is provided in the *ETX® Design Guide*. Refer to the documentation for additional information.

9.5.2 Battery

The implementation of the battery input complies with the *ETX® Specification*. Implementation information is provided in the *ETX® Design Guide*. Refer to the documentation for additional information.

In compliance with EN60950, there are at least two current-limiting devices (resistor and diode) between the battery and the consuming component.

9.5.3 I²C Bus

The I²C Bus is implemented by using general purpose I/O.

You also can access the I²C Bus via JUMPtec's Intelligent Device Architecture (JIDA) BIOS functions.

For additional information, refer to the *ETX® Design Guide*. I²C application notes and JIDA specifications which are available at the Kontron Web site.

9.5.4 SM Bus

System Management (SM) bus signals are connected to the SM bus controller, which is located in the southbridge (Intel 82801DB) device. For more information about the SM bus, please see the System Management (SM) Bus section in the Appendix A: System Resources chapter.

10 Special Features

10.1 Watchdog Timer

This feature is implemented in the Winbond 83627HF super I/O. You can configure the Watchdog Timer (WDT) in BIOS setup to start after a set amount of time after power-on boot. The WDT can also be controlled by the JIDA32 Library API (Refer to [Appendix F: JIDA Standard](#)). The application software should strobe the WDT to prevent its timeout. Upon timeout, the WDT resets and restarts the system. This provides a way to recover from program crashes or lockups.

Configuration

You can program the timeout period for the watchdog timer in two ranges:

- 1-second increments from 1 to 255 seconds
- 1-minute increments from 1 to 255 minutes

Contact Kontron Embedded Modules technical support for information on programming and operating the WDT.

11 Design Considerations

11.1 Thermal Management

A heat-spreader plate assembly is available from Kontron Embedded Modules for the *ETX®-P3T*. The heat-spreader plate on top of this assembly is NOT a heat sink. It works as an ETX®-standard thermal interface to use with a heat sink or other cooling device.

External cooling must be provided to maintain the heat-spreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heat-spreader plate temperature of 60° C or less.

The aluminum slugs and thermal pads on the underside of the heat-spreader assembly implement thermal interfaces between the heat spreader plate and the major heat-generating components on the *ETX®-P3T*. About 80 percent of the power dissipated within the module is conducted to the heat-spreader plate and can be removed by the cooling solution.

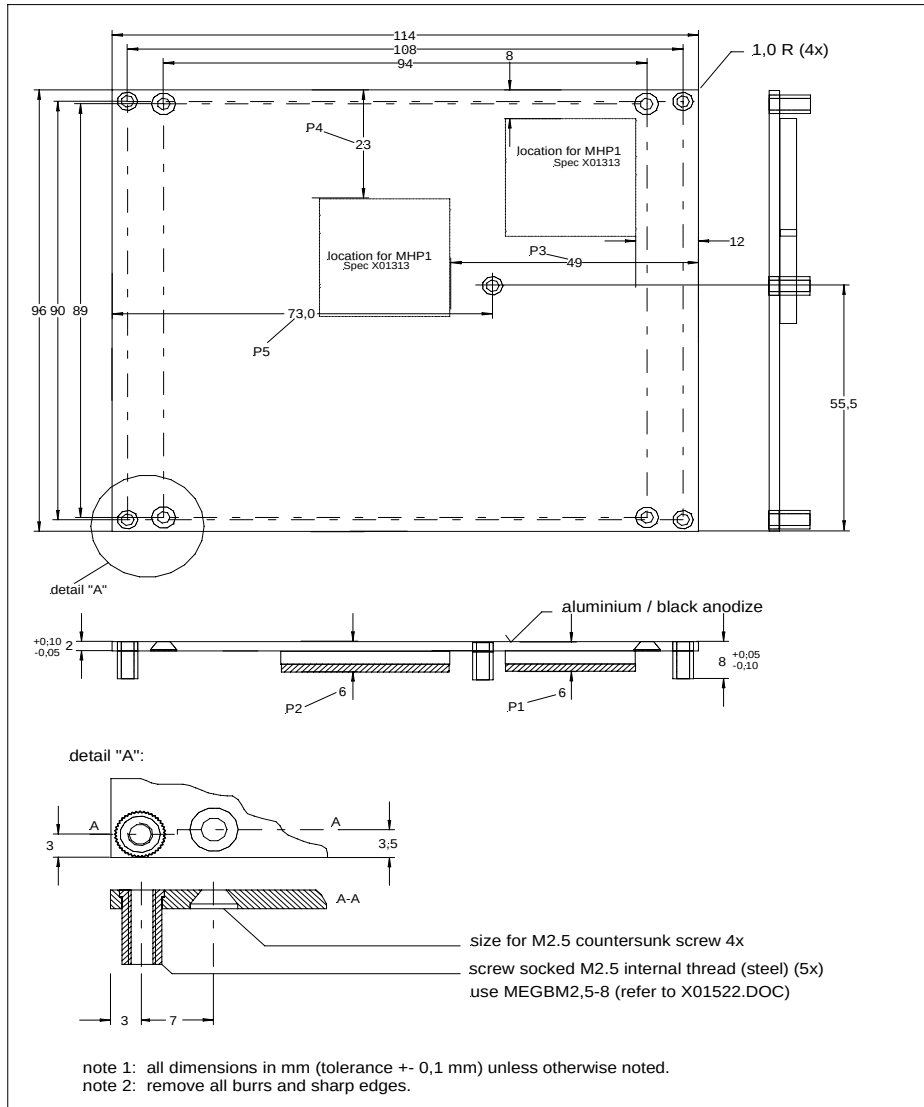
For 1000MHz modules, the heat dissipated into the plate ranges from 18 to 20 watts. Design a cooling solution to dissipate the heat load on a heat-spreader plate at a minimum of 20 watts to accommodate all *ETX®-P3T* modules.

You can use many thermal-management solutions with the heat-spreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the ETX® application and environmental conditions. Please see the *ETX® Design Guide* for further information on thermal management, or contact Kontron Embedded Modules technical support for help to design a solution that fits your system requirements.

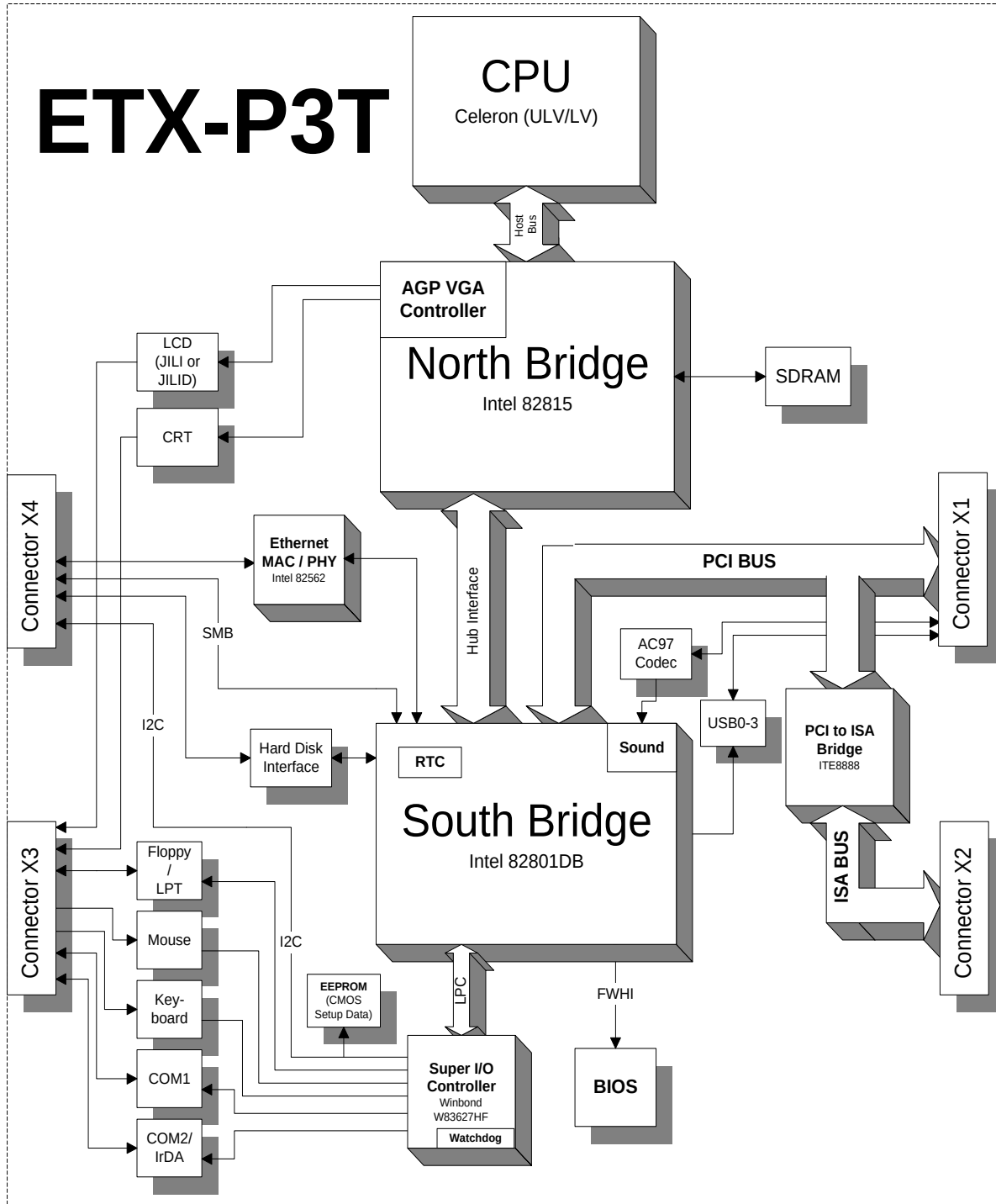
11.2 Heatspreader Dimensions

11.2.1 ETX®-P3T Heatspreader

This is the backside view of the heatspreader plate with pads marked for the heat generating components.



12 Appendix a: block diagram



13 Appendix B: Important Technology Information

The following technological information is designed to give the reader a better understanding of some of features of the ETX®-P3T. This information can be referenced when reading the “SYSTEM RESOURCES” and “BIOS OPERATION” sections that follow. There are also references to additional documentation that will help to develop a better understanding of the technical information described herein.

13.1 I/O APIC vs 8259 PIC Interrupt mode

The I/O APIC (Advanced Programmable Interrupt Controller) handles interrupts differently than the 8259 PIC. The following information explains these differences.

13.1.1 Method of interrupts transmission

The I/O APIC transmits interrupts through the system bus and interrupts are handled without the need for the processor to run an interrupt acknowledge cycle.

13.1.2 Interrupt priority

The priority of interrupts in the I/O APIC is independent of the interrupt number.

13.1.3 More interrupts

The I/O APIC in the chipset of the ETX®-P3T supports a total of 24 interrupts.

The APIC is not supported by all operating systems. Windows Xp and Win2k do support APIC. The APIC mode must be enabled in the BIOS setup before the OS installation. APIC only works in ACPI mode.

For more information see chapter 8 of the IA-32 Intel Architecture Software Developer's Manual, Volume 3.

Note: Enable the APIC mode if your OS supports it.

13.2 Native vs. compatible IDE mode

Windows XP SP1 and Windows Server 2003 will switch a native-mode-capable ATA controller from compatible to native mode if the BIOS indicates that the controller can be switched, the controller supports native mode and the appropriate registry key is set. The registry dword value `HKLM/CurrentControlSet/Control/PnP/Pci/ EnableNativeModeATA` must be added and set to any non 0 value.

13.2.1 Compatible Mode

The ATA controller emulates a legacy IDE controller, which is a non-standard extension of the ISA-based IDE controller. In compatible mode, the controller requires two ISA IRQs (14 and 15) that cannot be shared with other devices.

13.2.2 Native Mode

The ATA controller acts as a true PCI device that does not require dedicated legacy resources and can be configured anywhere in the system. ATA controllers running in native mode use their PCI interrupt for both channels and can share this interrupt pin with other devices in the system, like any other PCI device.

By requiring only one shareable interrupt instead of two non-shareable ones, native-mode controllers significantly decrease the likelihood that a user will install a device that cannot work because no interrupts are available.

Enable Native IDE mode if your OS supports it.

13.3 System Thermal Management

ACPI allows the OS to play a role in the thermal management of the system. With the OS in control of the operating environment, cooling decisions can be made based on the application load on the CPU and the thermal heuristics of the system.

The ACPI thermal solution on ETX®-P3T supports three cooling policies:

Active cooling

The OS is turning the fan on/off. Active cooling devices typically consume power and produce noise, but are able to cool a thermal zone without limiting system performance. The active cooling trip point declares the temperature threshold the OS uses to decide when to start/stop active cooling devices. See section [ETX®-P3T onboard Fan connector](#) for more information about the ETX®-P3T onboard Fan control.

Passive cooling

The OS reduces the power consumption of the processor by throttling the processor clock to reduce the temperature of the thermal zone. Passive cooling devices (processor) produce no noise. The passive cooling trip point declares the temperature threshold where the OS will start or stop passive cooling.

Critical Trip Point

The OS performs an orderly, but critical, shutdown of the system when the temperature reaches the critical trip point.

Summary

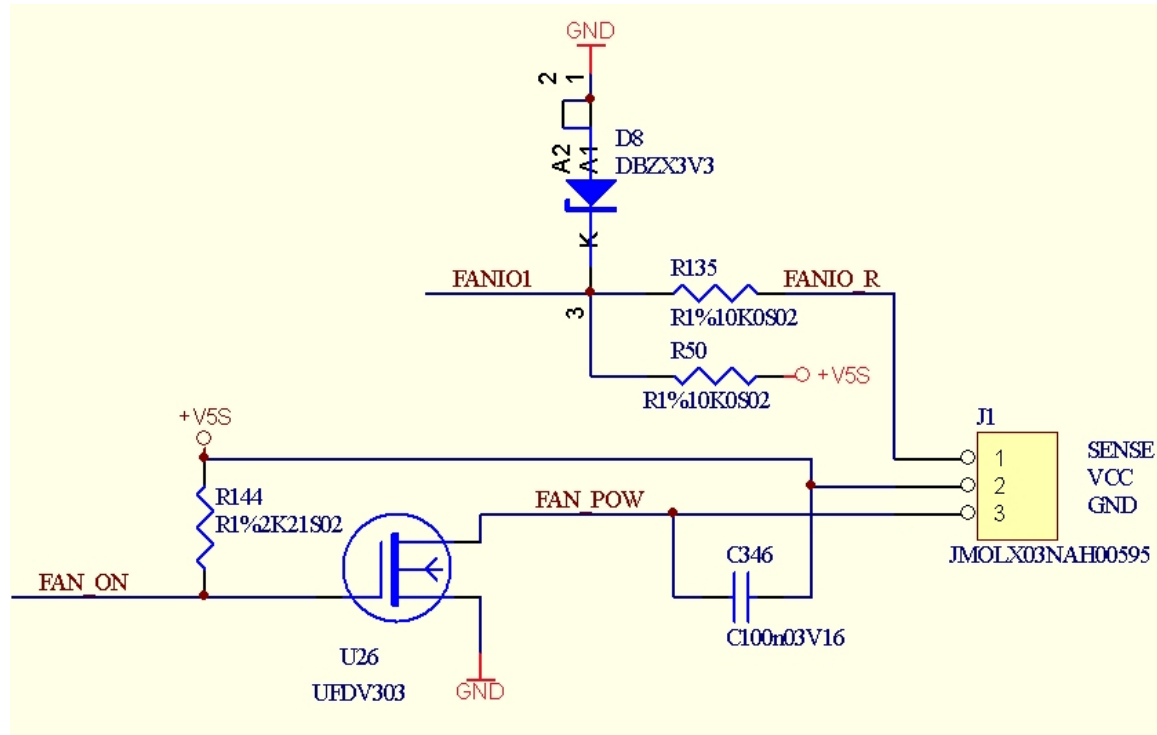
Thermal Control Circuit reduces performance when the processor reaches its max. operating temperature (100-110°C). THERMTRIP# shuts down the system in case of catastrophic cooling failure.

13.4 ETX®-P3T onboard Fan connector

This section describes how to connect a fan to the connector located directly on the ETX®-P3T. With certain BIOS-settings it is possible to control the fan depending on the Active Trip Point temperature. The fan switches on/off depending on the adjusted Active Trip Point temperature. In order for this feature to function properly an ACPI compliant OS is necessary.

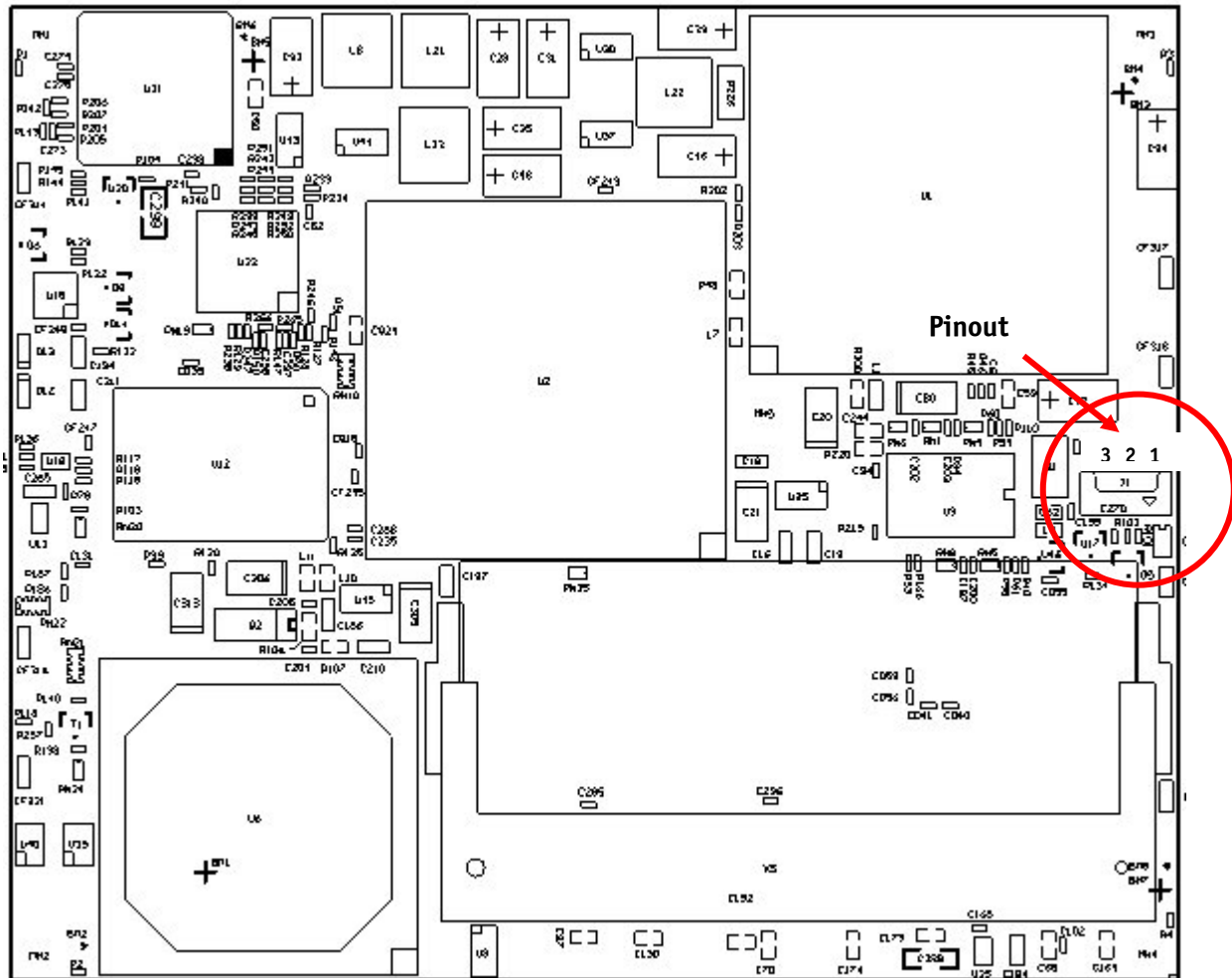
Note: The ETX®-P3T can not control the revolutions per minute (R.P.M) of the fan.

13.4.1 Schematics of Fan control



- Part number (Molex) J1: 53261-0390
- Mates with: 51021-0300
- Crimp terminals: 50079-8100

13.4.2 Location and Pinout of Fan connector J1



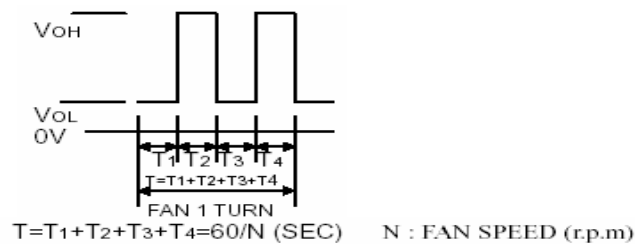
13.4.3 BIOS Settings

PhoenixBIOS Setup Utility					
M815	Main	Advanced	Security	Power	R115
					Exit
Enable ACPI: [Yes] ▶ ACPI Control Power Savings: [Disabled] Hard Disk Timeout: [Disabled] Resume On Modem Ring: [Off] Resume On Time: [Off] Resume Time: [00:00:00] Power supply: [ATX] Power Button Function: [Sleep]					Item Specific Help En/Disable ACPI BIOS (Advance Configuration and Power Interface)
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults Esc Exit Select Menu Enter Select ▶ Sub-Menu F10 Save and Exit					

M815 PhoenixBIOS Setup Utility R115	
Power	
ACPI Control	Item Specific Help
Active Trip Point: [80°C] Passive Cooling Trip Point: [Disabled] Critical Trip Point: [110°C] APIC - IO APIC Mode: [Disabled] Native IDE Support: [Disabled]	This value controls the temperature of the ACPI Active Trip Point - the point in which the OS will turn the CPU Fan on.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults Esc Exit Select Menu Enter Select ► Sub-Menu F10 Save and Exit	

13.4.4 Electrical characteristics

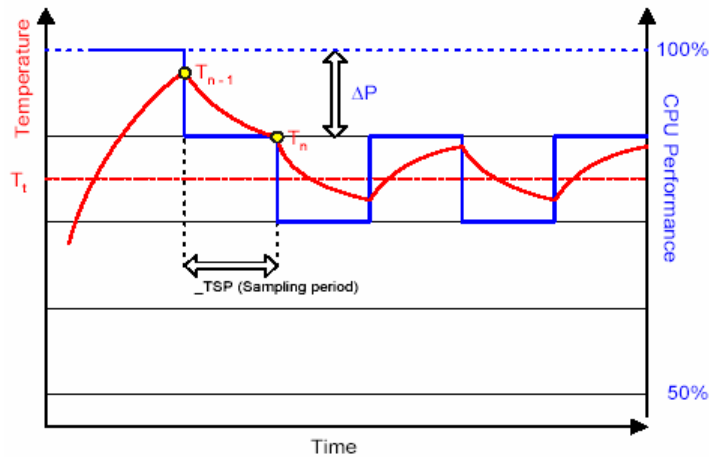
- $V_{cc} = 5\text{ V}$
- $I_{\max}(\text{continuous}) = 0,68\text{ A}$
- $I_{\max}(\text{pulsed}) = 2\text{ A}$
- Sense (Tacho-pulse) = 4 Pulses per turn



Note: The 5 V output is not short-circuit proof. The user has to ensure that the circuit is protected externally, for example by a fuse on the backplane.

13.5 Processor Clock Throttling

The ACPI OS assesses the optimum CPU performance change necessary to lower the temperature using the following equation:



$$\Delta P[\%] = TC1(T_n - T_{n-1}) + TC2(T_n - T_t)$$

ΔP is the performance delta, T_t is the target temperature = critical trip point. The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants the end user must supply (setup options section 15.6.1 ACPI Control Submenu).

It's up to the end user to set the cooling preference of the system by setting the appropriate trip points in the BIOS setup.

Note: See chapter 12 of the ACPI specification (www.acpi.info) for more details.

13.6 ACPI Suspend Modes and Resume Events

ETX®-P3T, only supports the S1 (POS=Power On Suspend) state. S3 (=Save to Ram) is not supported.

S4 (=Save to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems:

- WinME
- Win2k
- WinXP (S4_OS=Hibernate).

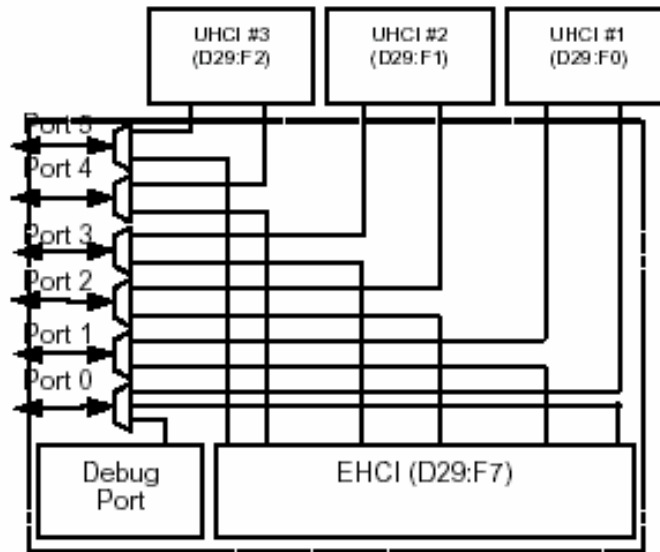
The following events resume the system from S1:

- Power Button
- PS/2 Keyboard and Mouse IRQs (1 & 12)
- USB Wake Events
- USB Keyboard and mouse activity
- PCI Bus signal PME#

13.7 USB 2.0 (EHCI) Host Controller Support

The EHCI host controller shares the 6 USB ports with the 3 UHCI host controllers. Integrated into the EHC functionality is a port-routing logic, which performs the mixing between the UHCI and EHCI host controllers. If a device is connected that is not capable of USB2.0's high-speed signaling protocol, or if the EHCI software drivers are not present, then the UHCI controller owns the ports.

Routing Diagram



Note: USB2.0 high-speed boot is supported by the BIOS.

14 Appendix C: System Resources

14.1 Interrupt Request (IRQ) Lines

In 8259 PIC mode

IRQ #	Used For	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Slave 8259	No	
3	COM2	No	Note (1)
4	COM1	No	Note (1)
5	LPT2	Yes	Note (2)
6	Floppy Drive Controller	No	Note (1)
7	LPT1	No	Note (1)
8	RTC	No	
9	SCI	Yes	Note (3)
10	COM3	Yes	Note (2)
11	COM4	Yes	Note (2)
12	PS/2 Mouse	No	Note (1)
13	FPU	No	
14	IDE0	No	Note (1)
15	IDE1	No	Note (1)

Notes: ¹ If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.

² Unavailable if baseboard is equipped with an I/O controller SMC FDC37C669, and the device is enabled in setup.

³ Unavailable in Advanced Configuration and Power Interface (ACPI) mode. Used as System Control Interrupt (SCI) in ACPI mode. The SCI is a shareable interrupt therefore IRQ9 can only be used for the PCI bus. It is not supported on the ISA bus.

In APIC mode:

IRQ #	Used For	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Slave 8259	No	
3	COM2	No	Note (1)
4	COM1	No	Note (1)
5	PCI/LPT2	Yes	Note (2)
6	Floppy Drive Controller	No	Note (1)
7	LPT1	No	Note (1)
8	RTC	No	
9	SCI	Yes	System Control Interrupt
10	COM3	Yes	Note (2)
11	COM4	Yes	Note (2)
12	PS/2 Mouse	No	Note (1)
13	FPU	No	

14	IDE0	No	Note (4)
15	IDE1	No	Note (4)
16	PIRQ[A]	For PCI	PCI IRQ line 1 + USB UCHI controller #1 + Graphics controller
17	PIRQ[B]	For PCI	PCI IRQ line 2 + AC97 Audio controller
18	PIRQ[C]	For PCI	PCI IRQ line 3 + USB UCHI controller #3 + Native IDE
19	PIRQ[D]	For PCI	PCI IRQ line 4 + USB UCHI controller #2
20	PIRQ[E]	No	Lan Controller
21	PIRQ[F]	No	
22	PIRQ[G]	No	
23	PIRQ[H]	No	USB EHCI controller

Notes: ¹ If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.

² Unavailable if baseboard is equipped with an I/O controller SMC FDC37C669, and the device is enabled in setup.

³ Unavailable in Advanced Configuration and Power Interface (ACPI) mode. Used as System Control Interrupt (SCI) in ACPI mode. The SCI is a shareable interrupt therefore IRQ9 can only be used for the PCI bus. It is not supported on the ISA bus.

⁴ IRQs are available if IDE controller is either disabled in setup or if in Native IDE mode.

14.2 Direct Memory Access (DMA) Channels

DMA #	Used for	Available	Comment
0		Yes	
1		Yes	Unavailable if Sound Blaster is enabled with default configuration.
2	FDC	No	If the "used-for" device is disabled in setup, the corresponding DMA channel is available for other devices.
3	LPT	Yes	Unavailable if LPT is used in ECP mode.
4	Cascade	No	
5		Yes	
6		Yes	
7		Yes	

14.3 Memory Area

Upper Memory	Used for	Available	Comment
C0000h – CFFFFh	VGA BIOS	No	
D0000h – DFFFFh		Yes	ISA bus or shadow RAM
E0000h – FFFFFh	System BIOS	No	

14.4 I/O Address Map

The I/O-port addresses of the ETX®-P3T are functionally identical with a standard PC/AT.

The following I/O ports are used:

I/O Address	Used for	Available	Comment
2E8-2EFh	COM4	No	Available if external I/O controller not used.
370-371h	Configuration space for SMC controller	No	Available if external I/O controller not used.
3E8-3EFh	COM3	No	Available if external I/O controller not used.

1000h >	PCI	No	I/O ports 1000h and above might be allocated by PCI devices or onboard hardware.
---------	-----	----	--

14.5 Peripheral Component Interconnect (PCI) Devices

PCI Device	Busmaster	PCI Interrupt	Comment
Audio, USB and Ethernet		See IRQ resource tables above	Integrated in the Intel chipset. No REQx/GNTx pair needed.

You can use REQ0/GNT0, REQ1/GNT1, REQ2/GNT2, and REQ3/GNT3 pairs for external PCI devices.

14.6 Inter-IC (I²C) Bus

I2C Address	Used For	Available	Comment	JIDA-Bus-Nr.
A0h	JIDA-EEPROM	No	EEPROM for CMOS data.	0
A2h	JIDA-EEPROM	No		0
B0h	WD-PIC	No	Reserved for internal use.	0

14.7 System Management (SM) Bus

Following SM bus addresses are reserved.

SM Bus Address	SM Device	Comment	JIDA-Bus-Nr.
10h	SMB host	Do not use under any circumstances.	1
12h	SMART_CHARGER	Not to be used with any SM bus device except a charger	1
14h	SMART_SELECTOR	Not to be used with any SM bus device except a selector	1
16h	SMART_BATTERY	Not to be used with any SM bus device except a battery	1
A0h	SPD	SDRAM EEPROM	1
D2h	Clock generator	Do not use under any circumstances.	1
60h	Reserved	Do not use	1

The standard ETX®-P3T Power management BIOS does not support batteries. If you require further information about this topic, please contact Kontron Embedded Modules Technical Support.

14.8 JILI-I²C Bus

I2C Address	Used For	Available	Comment	JIDA-Bus-Nr.
A0h	JILI-EEPROM	No	EEPROM for JILI-Data	2

15 Appendix D: BIOS Operation

The module is equipped with a Phoenix BIOS, which is located in an onboard Flash EEPROM. The device has 8-bit access. Faster access (16 bit) is provided by the shadow RAM feature. You can update the BIOS using a Flash utility.

15.1 Determining the BIOS Version

To determine the PhoenixBIOS version, immediately press the Pause key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

```
PhoenixBIOS 4.0 Release 6.1
Copyright 1985-2003 Phoenix Technology Ltd.
Kontron® BIOS Version <M815R115>
© Copyright 2007 Kontron Embedded Modules GmbH.
```

15.2 Setup Guide

The PhoenixBIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

The BIOS setup menus documented in this section represent those found in most models of the ETX®-P3T. The BIOS Setup for specific models can differ slightly.

Note: Selecting incorrect values may cause system boot failure. Load setup-default values to recover by pressing <F9>. It might also be necessary to use the "reset configuration data" option in the BIOS setup and set it to "yes". In certain circumstances this may also help to recover from system boot failure or a resource conflict.

15.2.1 Start Phoenix BIOS Setup Utility

To start the PhoenixBIOS setup utility, press <F2> when the following string appears during bootstrap.

Press <F2> to enter Setup

The Main Menu then appears.

The **Setup Screen** is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Bottom	Lists setup navigation keys.
Item Specific Help Window	Right	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.
General Help Window	Overlay (center)	Help for selected menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Tab> or <Shift-Tab>	Cycle cursor up and down.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F5> or <->	Select previous value for the current field.
<F6> or <+> or <Space>	Select next value for the current field.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The **Save Value** commands in the **Exit** menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (▶) marks all submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <F1> or <ALT-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

15.3 Main Menu

Feature	Option	Description
System Time	HH:MM:SS	Set system time. Use <Enter> to move to MM or SS.
System Date	MM/DD/YYYY	Set system date. Use <Enter> to move to DD or YYYY.
Legacy Diskette A	360 kB, 5 ¼ " 1.2 MB, 5 ¼ " 720 kB, 3 ½ " 1.44/1.25 MB, 3 ½ " 2.88 MB, 3 ½ " Disabled	Select type of floppy disk drive installed in system.

Legacy Diskette B	See above. Disabled	See above.
▸ Primary Master	Autodetected drive	Displays result of PM autotyping.
▸ Primary Slave	Autodetected drive	Displays result of PS autotyping.
▸ Secondary Master	Autodetected drive	Displays result of SM autotyping.
▸ Secondary Slave	Autodetected drive	Displays result of SS autotyping.
Smart Device Monitoring	Disabled Enabled	Turns on Self-Monitoring Analysis-Reporting Technology, which monitors the condition of the hard drive and reports when a catastrophic IDE failure is about to happen.
System Memory	N/A	Displays amount of conventional memory detected during bootup.
Extended Memory	N/A	Displays amount of extended memory detected during bootup.
BIOS Date	N/A	Displays the BIOS build Date

Note: In the Option column, bold shows default settings.

15.3.1 Master or Slave Submenus

Feature	Option	Description
Type	None IDE Removable ATAPI Removable CD-ROM Other ATAPI User Auto	None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. User = End user supplies the hdd information. Auto = Autotyping, the drive itself supplies the information. CD-ROM = CD-ROM drive.
Cylinders	1 to 65,536	Number of cylinders.
Heads	1 to 256	Number of read/write heads.
Sectors	1 to 63	Number of sectors per track.
Maximum Capacity	N/A	Displays the calculated size of the drive in CHS
Total Sectors	N/A	Number of total sectors in LBA mode
Maximum Capacity	N/A	Displays the calculated size of the drive in LBA
Multi-Sector Transfer	Disabled Standard 2 sectors 4 sectors 8 sectors 16 sectors	Any selection except Disabled determines the number of sectors transferred per block. Standard is 1 sector per block.
LBA Mode Control	Disabled Enabled	Enabling LBA causes Logical Block Addressing to be used in place of CHS.
32-Bit I/O	Disabled Enabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or Local Bus.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3/ DMA 1 FPIO 4/ DMA 2	Selects the method for transferring the data between the hard disk and system memory.
Ultra DMA Mode	Disabled Mode 0	Selects the UDMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.

	Mode 1 Mode 2 Mode 3 Mode 4 Mode 5	
SMART Device Monitoring	Disabled Enabled	Shows if SMART Device monitoring is supported by the drive.

15.4 Advanced Menu

Feature	Option	Description
▸ Advanced Chipset Control	sub menu	Opens Advanced Chipset Control sub menu.
▸ PCI/PNP Configuration	sub menu	Opens PCI/PNP Config sub menu.
▸ Memory Cache	sub menu	Opens Cache Control sub menu.
▸ I/O Device Configuration	sub menu	Opens Peripheral Config sub menu.
▸ Keyboard Features	sub menu	Opens Keyboard Features sub menu.
▸ Hardware Monitor	sub menu	Shows hardware monitor current state.
▸ Watchdog Settings	sub menu	Opens Watchdog Config sub menu.
▸ Display Control	sub menu	Opens Display Control sub menu
▸ Miscellaneous	sub menu	Opens sub menu with miscellaneous options.

15.4.1 Advanced Chipset Control Submenu

Feature	Option	Description
Video Boot type	Disabled Onboard Video Onboard Video 512k Onboard Video 1MB	Select 'Onboard Video' to enable the onboard video controller as the boot display device. Either 512kB or 1MB of system memory can be allocated for VGA UMA. If the onboard video controller is disabled no system memory will be allocated for video.
Enable Memory gap	Disabled Enabled	Allows enabling a 1MB memory gap for add-on cards at 15MB

Note: In the Option column, bold shows default settings.

15.4.2 PCI/PNP Configuration Submenu

Feature	Option	Description
Plug & Play OS	No Yes	If your system has a PnP OS (e.g. Win9x) select Yes to let the OS configure PnP devices not required for booting. No allows the BIOS to configure them.
Reset Configuration Data (*)	No Yes	Yes erases all configuration data in ESCD, which stores the configuration settings for plug-in devices. Select Yes when required to restore the manufacturer's defaults.
Secured Setup Configuration	Yes No	Yes prevents a Plug and Play OS from changing system settings.
▸ PCI Device, Slot #x	sub menu	Opens sub menu to configure slot x PCI device
PCI IRQ line 1 PCI IRQ line 2 PCI IRQ line 3 PCI IRQ line 4 Onboard LAN IRQ line	Disabled Auto IRQ3, 4, 5, 7, 9, 10, 11, 12, 14, 15	Select IRQs for external PIC interrupts A/B/C/D and the onboard LAN and USB2.0 host controller. Select Auto to let the BIOS assign the IRQ.

Onboard EHCI IRQ line		
▸ PCI/PNP ISA IRQ Resource Exclusion	sub menu	Opens IRQ Exclusion sub menu.
Assign IRQ to SMB	Disabled Enabled	Determines whether the onchip SMBus host controller gets an IRQ assigned

Notes: In the Option column, bold shows default settings.

() Setting this option to "yes", under certain circumstances, may help to recover from system boot failure or a resource conflict.*

15.4.3 PCI Device, Slot # x Submenu

Feature	Option	Description
Option ROM Scan	Disabled Enabled	Initialize device expansion ROM.
Enable Master	Disabled Enabled	Enables device in slot as a PCI bus master, not every device can function as a master. Check device documentation.
Latency Timer	20h, 40h , 60h, 80h, A0h, C0h, E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks. A high-priority, high-throughput device may benefit from a greater value.

Note: In the Option column, bold shows default settings.

15.4.4 PCI/PNP ISA IRQ Exclusion Submenu

Feature	Option	Description
IRQ3	Available Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ4	see above	see above
IRQ5	see above	see above
IRQ7	see above	see above
IRQ9*	Reserved	Used for SCI in ACPI mode. Do not use for legacy ISA devices.
IRQ10	see above	see above
IRQ11	see above	see above
IRQ12	see above	see above
IRQ14	see above	see above (visible only if primary IDE disabled)
IRQ15	see above	see above (visible only if secondary IDE disabled)

Note: In the Option column, bold shows default settings.

**IRQ9 is used for SCI in ACPI mode. Do not use for legacy ISA devices.*

15.4.5 Memory Cache Submenu

Feature	Option	Description
Memory Cache	Disabled Enabled	Enables or Disables the L2 cache.
Cache System BIOS area	uncached	Controls caching of system BIOS area.

	Write Protected	
Cache Video BIOS area	uncached Write Protected	Controls caching of system BIOS area.
Cache Extended Base / Extended Memory area:	uncached Write Through Write Protected Write Back	Controls caching of system memory below 640k / above 1MB.
D000 – D3FF D400 – D7FF D800 – DBFF DC00 – DFFF	Disabled Write Through Write Protected Write Back	Disabled: block is not cached. Write Through: Writes are cached and sent to main memory at once. Write Protect: Writes are ignored. Write Back: Writes are cached, but not sent to main memory until necessary.

Notes: In the Option column, bold shows default settings.

15.4.6 I/O Device Configuration Submenu

Feature	Option	Description
Local Bus IDE adapter	Disabled Primary Secondary Both	Enables onboard PCI IDE device.
USB UHCI Host Controller 1	Enabled Disabled	Enable/ Disable UHCI 1 HC = USB ports 0 and 1.
Primary IDE UDMA66/100	Disabled Enabled	Disabled limits max. transfer mode to UDMA33. Enabled allows UDMA66 and above.
Secondary IDE UDMA66/100	Disabled Enabled	See above.
USB UHCI Host Controller 1	Enabled Disabled	Enable/ Disable UHCI 1 HC = USB ports 0 and 1.
USB UHCI Host Controller 2	Enabled Disabled	Enable/ Disable UHCI 2 HC = USB ports 2 and 3.
USB EHCI Host Controller **	Disabled Enabled	Controls USB 2.0 functionality.**
Legacy USB Support	Disabled Enabled	Enable support for USB keyboard and mice and boot from USB mass storage devices.
AC97 Audio Controller	Disabled Enabled	Enable the AC97 Audio device.
Onboard LAN Controller	Disabled Enabled	Enables the ICH4 internal LAN controller.
Onboard LAN PXE ROM	Disabled Enabled	Enables the remote boot BIOS extension for the onboard LAN controller.
*Onboard FDC	Disabled Enabled	Enables the onboard FDC controller.
Serial port A	Disabled	Disabled turns off the port.

Serial port B	Enabled Auto OS Controlled	Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port. OS Controlled lets the PnP OS configure the port after bootup.
Mode	Normal , IrDA	Set the mode for serial port B.
Base I/O address	3F8h, 2F8h, 3E8h, 2E8h	Select I/O base of port.
IRQ (port A and B)	IRQ 3, IRQ 4	Select IRQ of port A and B
*Onboard LPT	Disabled Enabled Auto	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port.
*Mode	Output only Bi-directional EPP ECP	Set the mode for the parallel port.
*Base I/O address	378h , 278h, 3BCh	Select I/O base of port.
*IRQ	IRQ 5, IRQ 7	Select IRQ of parallel port.
*DMA	DMA1, DMA3	Select DMA channel of port if in ECP mode.

Notes: In the Option column, bold shows default settings.

The FDC and LPT settings marked with an asterisk (*) are mutually exclusive. The FDC or the LPT settings are visible, depending on a configuration resistor on the OEM backplane. If FDC is selected, the FDC signals are available at the LPT port (external floppy). Only Drive B (MOD1/DRV1) is supported, but the drives are internally swapped to let the drive appear as Drive A.

**The USB ports are multiplexed between UHCI and EHCI. Ports are routed to EHCI if an USB 2.0 high-speed device is connected and an EHCI driver is loaded.

If you want to use the USB boot feature, enable USB BIOS Legacy Support.

15.4.7 Keyboard Features Submenu

Feature	Option	Description
Numlock	Auto On Off	On or Off turns NumLock on or off at bootup. Auto turns NumLock on if it finds a numeric key pad.
Key Click	Disabled Enabled	Turns audible key click on.
Keyboard auto-repeat rate	30/sec , 26.7/sec, 21.8/sec, 13.3/sec, 10/sec, 6/sec, 2/sec	Sets number of times to repeat a keystroke per second if you hold the key down.
Keyboard auto-repeat delay	¼ sec, ½ sec , ¾ sec, 1 sec	Sets delay time after the key is held down before it begins to repeat the keystroke.

Note: In the Option column, bold shows default settings.

15.4.8 Hardware Monitor Submenu

This submenu shows the current voltages and temperatures of the system.

	3.3V power plane
CPU core	Core voltage (depends on CPU)
5Vsb	5V Standby plane
V(5)	5V power plane
Battery	Backup battery voltage
CPU Temp	Temperature of CPU die

15.4.9 Watchdog Settings Submenu

Feature	Option	Description
Mode	Disabled Reset	Select watchdog operation mode.
Delay	1s, 5s, 10s, 30s , 1min, 5min, 10min, 30min	The time until the watchdog counter starts counting. Useful to handle longer boot times.
Timeout	0.4s, 1s, 5s, 10s, 30s , 1min, 5min, 10min	Maximum trigger period.

Note: In the Option column, bold shows default settings.

15.4.10 Display Control Submenu

Feature	Option	Description
Display Mode	CRT only LCD only CRT+LCD	Select the display mode.
JDA Revision	N/A	Displays the revision of the JILI data area image.
Flat Panel Type	VGA SVGA XGA XGA2 SXGA UXGA Enter PAID Enter FPID Auto	Select Auto to let the BIOS automatically detect the panel type or use one of the predefined fixed panel types. Choose Enter PAID or Enter FPID to manually set JILI3 ID values.
PAID/FPID ¹	0 – FFFF, default 0	Enter the JILI3 ID.
Flat Panel Backlight ²	0 – 255, default 128	Enter a value to adjust backlight of the LCD.
Flat Panel Contrast ³	0 – 63, default 32	Enter a value to adjust contrast of the LCD.
Default Primary Video Adapter	PCI AGP	Select PCI or AGP to have a PCI Video Card or AGP Video Card, If installed, used for the Boot display device
Assign IRQ to VGA	Yes No	Determines whether the VGA Device gets an IRQ assigned

Notes: ¹Only available if Flat Panel Type (Enter PAID) or (Enter FPID) are selected.

²Only available if the DAC (MAX5362) is on the OEM backplane or the panel adapter.

³ Only available if the digitally controlled potentiometer (Xicor X9429) is on the OEM backplane or the panel adapter

15.4.11 Miscellaneous Submenu

Feature	Option	Description
Floppy Check	Disabled Enabled	Enabled verifies floppy type on boot; disabled speeds boot.
Summary Screen	Disabled Enabled	If enabled, a summary screen is displayed just before booting the OS to let the end user see the system configuration.
QuickBoot Mode	Disabled Enabled	Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
Extended Memory Testing	<i>Normal</i> Just zero it None	Determines which type of tests will be performed on memory above 1MB. <i>The option Normal is not visible if QuickBoot is enabled.</i>
Dark Boot	Disabled Enabled	If enabled, system comes up with a blank screen instead of the diagnostic screen during startup.
Halt On Errors	Yes No	Determines if post errors cause the system to halt.
PS/2 Mouse	Autodetect Enabled Disabled	Selecting Disabled prevents any installed PS/2 mouse from functioning, but frees up IRQ12. Selecting Autodetect frees IRQ12 if no mouse was detected.
Large Disk Access Mode	DOS Other	Select DOS if you have DOS. Select Other if you have another OS such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads or more than 63 sectors per track.
Spread Spectrum	Disabled Enabled	Controls the Spread Spectrum feature of the clock generator

15.5 Security Menu

Feature	Option	Description
Set User Password	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives restricted access to setup.
Set Supervisor Password	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives full access to setup.
Password on boot	Disabled Enabled	Enabled requires a password on boot. Requires prior setting of the supervisor password. If supervisor password is set and this option is disabled, BIOS assumes user is booting.
Diskette access	User Supervisor	Enabled requires supervisor password to access floppy disk.
Fixed disk boot sector	Normal Write protected	Write protect the boot sector on the hard disk for virus protection. Requires a password to format or Fdisk the hard disk.
Virus check reminder System backup reminder	Disabled Daily Weekly Monthly	Displays a message during bootup asking (Y/N) if you backed up the system or scanned for viruses. Message returns on each boot until you respond with „Y“. Daily displays the message on the first boot of the

	day, Weekly on the first boot after Sunday, and Monthly on the first boot of the month.
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Notes: In the Option column, bold shows default settings.
 Enabling Supervisor Password requires a password for entering Setup.
 Passwords are not case sensitive.
 User and Supervisor passwords are related.
 A User password is possible only if a Supervisor password exists.

15.6 Power Menu

A power management system reduces the amount of energy used after specified periods of inactivity. The setup menu supports:

- Full On state
- Standby state with partial power reduction
- Suspend state with full power reduction

Use the **Advanced Options** menu to specify whether an activity can terminate a Standby or Suspend state and restore Full On.

Feature	Option	Description
*Enable ACPI	No Yes	Enables/Disables ACPI BIOS (Advanced Configuration and Power Interface). IRQ9 is used for SCI (System Control Interrupt). Do not use for ISA bus devices.
*Thermal Management	Sub Menu (available only if Enable ACPI = No)	Opens the thermal management sub menu
ACPI Control	sub menu	Opens the ACPI sub menu
Power Savings	Disabled Customized Maximum Power Saving Maximum Performance	Maximum options select predefined values. Select Customized to make your own selections from the following fields. Disabled turns off all power management.
Standby Timeout	Off , 1min, 2min, 4min, 8min	Inactivity period required to put system in Standby mode (partial power shutdown).
Auto Suspend Timeout	Off , 5min, 10min, 15min, 20min, 30min, 40min, 60min	Inactivity period required after Standby to Suspend mode (maximum power shutdown).
Hard Disk Timeout	Disabled , 10 sec – 15 min	Inactivity period of hard disk required before standby (motor off).
Video Timeout	Disabled , 10 sec – 15 min	Inactivity period of user input device before the screen is turned off.
Resume on Modem Ring	Off On	Enabled wakes the system on incoming calls detected by mode (RI).
Resume on Time	Off On	Enabled wakes the system at a specific time.
Resume Time	00:00:00	Specifies the time when the system is to wake.
Power Button Function	Power Off Sleep	Determines if the system enters suspend or soft off when the power button is pressed.
Power Loss Control	Stay Off Power On Last State	Determines how the system behaves after a power failure. This only works in conjunction with a CMOS backup battery.

*Notes: In the Option column, bold indicates default setting.
See section 13 of this user's guide for more details about ACPI.*

15.6.1 ACPI Control Submenu

Feature	Option	Description
Active Trip Point	Disabled 40°C – 100°C	Determines the temperature of the ACPI Active Trip Point, the point at which the OS will turn on/off the CPU fan.
Passive Trip Point	Disabled 40°C – 100°C	Determines the temperature of the ACPI Passive Trip Point, the point at which the OS will turn on/off CPU clock throttling.
Passive TC1 Value	1 , 2, 3, ...15, 16	Determines the TC1 (temperature coefficient 1) value for the ACPI passive cooling formula. See section 13.4 for more details.
Passive TC2 Value	1, 2, 3, 4, 5 , ...15, 16	Determines the TC2 (temperature coefficient 2) value for the ACPI passive cooling formula. See section 13.4 for more details.
Passive TSP Value	2, 4, 6, 8, 10 , ... 28, 30	Determines the Tsp (sampling period) value for the ACPI passive cooling formula. See chapter 13.4 below for more details.
Critical Trip Point	40°C – 110°C	This value controls the temperature of the ACPI Critical Trip Point- the point at which the OS will shut the system off.
APIC – IO APIC Mode	Disabled Enabled	This item is valid only for Windows XP. Also, a fresh install of the OS must occur when APIC Mode is desired Test the IO APIC by setting an item to Enabled. The APIC Table will then be pointed to by the RSDT, the Local APIC will be initialized, and the proper enable bits will be set in IHC4M. See section 13.1
Native IDE Support	Disabled Enabled	Enable Native IDE support for WINXP by setting this item. The NATA Package will be created if this item is set to Enabled. Changing this item will have no effect in WIN98, WINME, or WIN2K. See section 13.2 for more details.

15.6.2 ACPI Resume Events

ETX®-P3T supports S1 state only, no S3 (S2R) and S4 (S2D). The following events resume the system from S1:

- Power button
- PCI bus signal PME#
- PS/2 keyboard and mouse
- USB keyboard and mouse activity
- USB resume event

15.6.3 Thermal Management Submenu

Available only if Enable ACPI = No selected

Feature	Option	Description
Auto Thermal Throttling	Enabled Disabled	Reduces CPU Speed to overheating
Temperature	75°C, 80°C, ..., 100°C , 105°C, 110°C	CPU clock Throttling starts when reaching this temperature given in degrees Celsius
Hysteresis	3°C, 4°C, 5°C , 6°C	Amount of degrees the temperature must decrease before CPU clock gets restore to 100% again.
CPU Performance	13%, 25%, 50% , 75%	The CPU performance will be reduced to the selected value when reaching the temperature threshold.

15.7 Boot Menu

15.7.1 MultiBoot

Multiboot allows you to select the following boot devices:

- Hard disk
- Floppy disk
- CD-ROM
- Network card

You can make the selections from Setup, or by selecting the boot device in the BootFirst Menu.

Note: ETX®-P3T also supports booting from USB floppy and Mass Storage Device (MSD).

MultiBoot consists of the 2 menus:

- Setup Boot Menu
- Boot First Menu

15.7.2 The Setup Boot Menu

This menu allows selecting the order of the devices from which the BIOS attempts to boot the OS. During POST, if BIOS is unsuccessful at booting from one device, it will try the next one on the list. The Boot Menu shows two lists, the boot priority list and the exclude from boot order list. The sample below shows the default configuration.

Boot Priority order:	Item Specific Help
IDE0: <primary master device> IDE1: <primary slave device> IDE2: <secondary master device> IDE3: <secondary slave device> IDE CD <IDE CD-ROM> USB Key: <USB stick> USB CD: <USB CD-ROM>	Keys used to view or configure devices: Up and Down arrows select a device. <+> and <-> moves the device up or down. <f> and <r> specifies the device fixed or removable. <x> exclude or include the device to boot. <Shift + 1> enables or disables a device. <1 – 4> Loads default boot sequence.
Exclude from boot order:	

USB CDROM: <USB Floppy device>	
USB HDD: <USB hard disk>	
USB ZIP: <USB zip device>	
USB LS-120: <USB CDROM device>	
PCI LAN: <PCI LAN device>	
PCI SCSI: <PCI SCSI device>	
Bootable Add-in Cards <like PCMCIA and older SCSI adapters>	

*Notes: The standard 1.44MB floppy drive is referenced as Legacy Floppy Drives.
The BIOS only tries to boot from the devices (max 8) in the Boot Priority Order list.*

15.7.3 Boot First Menu

Display the **Boot First Menu** by pressing <Esc> during POST. In response, the BIOS displays the message Entering Boot Menu and then displays the Boot Menu at the end of POST.

Use the menu to select one of the following options:

- Override the existing boot sequence (for this boot only) by selecting another boot device. If the specified device does not load the OS, the BIOS reverts to the previous boot sequence.
- Enter Setup.
- Press <Esc> to continue with the existing boot sequence.

15.8 Exit Menu

The following sections describe the five options in **Exit Menu**. Pressing <Esc> does not exit this menu. You must select an item from the menu to exit.

Exit Saving Changes

Saves all selections and exits setup. Upon reboot, the BIOS configures the system according to the Setup selection stored in CMOS.

Exit Discarding Changes

Use this option to exit Setup without storing new selections in CMOS. Previous selections remain in effect.

Load Setup Defaults

Select to display the default values for all Setup menus.

Discard Changes

Discards changes made during a Setup session and revert to values previously saved in CMOS.

Save Changes

Saves all selections without exiting Setup.

15.9 Updating or Restoring BIOS

Phoenix Phlash16 allows you to update or restore the BIOS with a newer version or restore a corrupt BIOS by using a floppy disk without having to install a new ROM chip.

- Get the Phoenix Phlash16 compressed file, CRDxM815.ZIP, from the Kontron Embedded Modules. It contains the following files:

File	Purpose
MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette.
CRISBOOT.BIN	Serves as the Crisis Recovery boot sector code.
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH16.EXE	Programs the Flash ROM.
WINCRISIS.EXE	Creates the Crisis Recovery Diskette from Windows.
WINCRISIS.HLP	Serves as the help file of WINCRISIS.EXE.
BIOS.WPH	Serves as the actual BIOS image to be programmed into Flash ROM.

BIOS.WPH is a file that contains the 1MB BIOS binary and flash interface code required by Phlash16.EXE

- To install Phoenix Phlash16 on a hard disk, unzip the content of CRDxM815.ZIP into a local directory such as C:\PHLASH.

Note: Crisis Recovery requires either a floppy disk connected to the LPT interface (external floppy drive_1) or an USB floppy drive.

- To create a Crisis Recovery Diskette, insert a blank diskette into Drive A: or B: and execute WINCRISIS.EXE. This copies four files onto the Crisis Recovery Diskette.

File	Purpose
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH16.EXE	Programs the Flash ROM.
BIOS.WPH	Serves as the BIOS image to be programmed into Flash ROM.

- If the BIOS image (BIOS.WPH) changes because of an update or bug fix, copy the new BIOS.WPH image onto the diskette.
- Phoenix Phlash16 runs in one of two modes: Command Line or Crisis Recovery. Use the Command Line mode to update or replace a BIOS. To execute Phlash16 in this mode, move to the Crisis Recovery Disk and type PHLASH16. Phoenix Phlash16 will update the BIOS. Phlash16 can fail if the system uses memory managers. If this occurs, the utility displays the following message:

Cannot flash when memory managers are present.
- If you see this message after you execute Phlash16, disable the memory manager or use parameter /x for Phlash16.exe.

15.10 Preventing Problems When Updating or Restoring BIOS

Updating the BIOS represents a potential hazard. Power failures or fluctuations that may occur during updating the Flash ROM can damage the BIOS code, making the system unbootable.

To prevent this potential hazard, many systems come with a boot-block Flash ROM. The boot-block region contains a fail-safe recovery routine. If the boot-block code finds a corrupted BIOS (checksum fails), it boots into the crisis recovery mode and loads a BIOS image from a crisis diskette (see above).

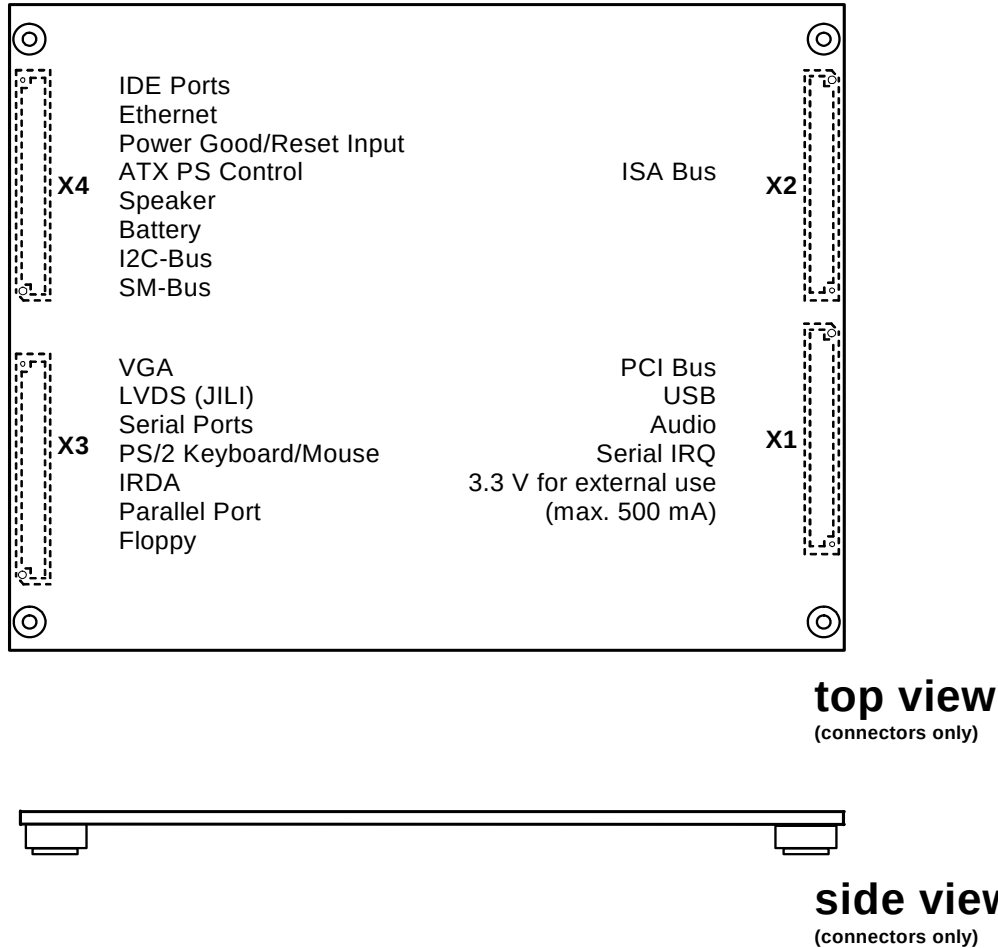
Additionally, the end user can insert an update key into the serial port (COM1 only) to force initiating the recovery routine for the boot block.

For further information on the update key and the crisis diskette, see application note Phlash_EC_E1xx.pdf, which is available from the Kontron Web site (<http://emea.kontron.com>).

16 Appendix E: ETX® Connector Pinouts

The pinouts for ETX® Interface Connectors X1, X2, X3, and X4 are documented for convenient reference. Please see the *ETX® Specification* and *ETX® Design Guide* for detailed, design-level information.

16.1 Connector Locations



16.2 Signal Description

Term	Description
I0-3,3	Bi-directional 3,3 V I0-Signal
I0-5	Bi-directional 5 V I0-Signal
I-3,3	3,3 V Input
I-5	5 V Input
O-3,3	3,3 V Output
O-5	5 V Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection
nc	Not Connected / Reserved

16.3 Connector X1 (PCI Bus, USB, Audio)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC *	52	VCC *
3	PCICLK3	4	PCICLK4	53	PAR	54	SERR#
5	GND	6	GND	55	GPERR#	56	RESERVED
7	PCICLK1	8	PCICLK2	57	PME#	58	USB2#
9	REQ3#	10	GNT3#	59	LOCK#	60	DEVSEL#
11	GNT2#	12	3V	61	TRDY#	62	USB3#
13	REQ2#	14	GNT1#	63	IRDY#	64	STOP#
15	REQ1#	16	3V	65	FRAME#	66	USB2
17	GNT0#	18	RESERVED	67	GND	68	GND
19	VCC *	20	VCC *	69	AD16	70	CBE2#
21	SERIRQ	22	REQ0#	71	AD17	72	USB3
23	AD0	24	3V	73	AD19	74	AD18
25	AD1	26	AD2	75	AD20	76	USB0#
27	AD4	28	AD3	77	AD22	78	AD21
29	AD6	30	AD5	79	AD23	80	USB1#
31	CBE0#	32	AD7	81	AD24	82	CBE3#
33	AD8	34	AD9	83	VCC *	84	VCC *
35	GND	36	GND	85	AD25	86	AD26
37	AD10	38	AUXAL	87	AD28	88	USB0
39	AD11	40	MIC	89	AD27	90	AD29
41	AD12	42	AUXAR	91	AD30	92	USB1
43	AD13	44	ASVCC	93	PCIRST#	94	AD31
45	AD14	46	SNDL	95	INTC#	96	INTD#
47	AD15	48	ASGND	97	INTA#	98	INTB#
49	CBE1#	50	SNDR	99	GND	100	GND

Notes: *To protect external power lines of peripheral devices, make sure that:
the wires have the right diameter to withstand the maximum available current
the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950

16.3.1 Connector X1 (Signal Levels)

Pin 1-50: PCI|USB|AUDIO

Pin	Signal	Description	Type	Termination	Comment
1	GND	Ground	PWR	-	-
2	GND	Ground	PWR	-	-
3	PCICLK3	PCI Clock Slot 3	O-3,3	-	-
4	PCICLK4	PCI Clock Slot 4	O-3,3	-	-
5	GND	Ground	PWR	-	-
6	GND	Ground	PWR	-	-
7	PCICLK1	PCI Clock Slot 1	O-3,3	-	-
8	PCICLK2	PCI Clock Slot 2	O-3,3	-	-
9	REQ3#	PCI Bus Request 3	I-3,3	PU 8k2 3,3V	-
10	GNT3#	PCI Bus Grant 3	O-3,3	-	-
11	GNT2#	PCI Bus Grant 2	O-3,3	-	-
12	3V	Power +3,3V	PWR	-	-
13	REQ2#	PCI Bus Request 2	I-3,3	PU 8k2 3,3V	-
14	GNT1#	PCI Bus Grant 1	O-3,3	-	-
15	REQ1#	PCI Bus Request 1	I-3,3	PU 8k2 3,3V	-
16	3V	Power +3,3V	PWR	-	-
17	GNT0#	PCI Bus Grant 0	O-3,3	-	-
18	nc	-	nc	-	Reserved
19	VCC	Power +5V	PWR	-	-
20	VCC	Power +5V	PWR	-	-
21	SERIRQ	Serial Interrupt Request	IO-3,3	PU 8k2 3,3V	-
22	REQ0#	PCI Bus Request 0	I-3,3	PU 8k2 3,3V	-
23	AD0	PCI Address & Data Bus line	IO-3,3	-	-
24	3V	Power +3,3V	PWR	-	-
25	AD1	PCI Address & Data Bus line	IO-3,3	-	-
26	AD2	PCI Address & Data Bus line	IO-3,3	-	-
27	AD4	PCI Address & Data Bus line	IO-3,3	-	-
28	AD3	PCI Address & Data Bus line	IO-3,3	-	-
29	AD6	PCI Address & Data Bus line	IO-3,3	-	-
30	AD5	PCI Address & Data Bus line	IO-3,3	-	-
31	CBE0#	PCI Bus Command and Byte enables 0	IO-3,3	-	-
32	AD7	PCI Address & Data Bus line	IO-3,3	-	-
33	AD8	PCI Address & Data Bus line	IO-3,3	-	-
34	AD9	PCI Address & Data Bus line	IO-3,3	-	-
35	GND	Ground	PWR	-	-
36	GND	Ground	PWR	-	-
37	AD10	PCI Address & Data Bus line	IO-3,3	-	-
38	AUXAL	Auxiliary Line Input Left	I	-	4k7 Ohm Resistors
39	AD11	PCI Address & Data Bus line	IO-3,3	-	-
40	MIC	Microphone Input	I	-	-
41	AD12	PCI Address & Data Bus line	IO-3,3	-	-
42	AUXAR	Auxiliary Line Input Right	I	-	4k7 Ohm Resistors
43	AD13	PCI Address & Data Bus line	IO-3,3	-	-
44	ASVCC	Analog Supply of Sound Controller	O-5	-	-
45	AD14	PCI Address & Data Bus line	IO-3,3	-	-
46	SNDL	Audio Out Left	O	-	-
47	AD15	PCI Address & Data Bus line	IO-3,3	-	-
48	ASGND	Analog Ground of Sound Controller	PWR	-	-
49	CBE1#	PCI Bus Command and Byte enables 1	IO-3,3	-	-
50	SNDR	Audio Out Right	O	-	-

Pin 51–100: PCI | USB | AUDIO

Pin	Signal	Description	Type	Termination	Comment
51	VCC	Power +5V	PWR	-	-
52	VCC	Power +5V	PWR	-	-
53	PAR	PCI Bus Parity	IO-3,3	-	-
54	SERR#	PCI Bus System Error	IO-3,3	PU 8k2 3,3V	-
55	GPERR#	PCI Bus Grant Error	IO-3,3	PU 8k2 3,3V	-
56	nc	-	nc	-	Reserved
57	PME#	PCI Power Management Event	IO-3,3	-	int. PU 20k 3,3V in ICH4
58	USB2#	USB Data- , Port2	IO-3,3	-	int. PD 15k in ICH4
59	LOCK#	PCI Bus Lock	IO-3,3	PU 8k2 3,3V	-
60	DEVSEL#	PCI Bus Device Select	IO-3,3	PU 8k2 3,3V	-
61	TRDY#	PCI Bus Target Ready	IO-3,3	PU 8k2 3,3V	-
62	USB3#	USB Data- , Port3	IO-3,3	-	int. PD 15k in ICH4
63	IRDY#	PCI Bus Initiator Ready	IO-3,3	PU 8k2 3,3V	-
64	STOP#	PCI Bus Stop	IO-3,3	PU 8k2 3,3V	-
65	FRAME#	PCI Bus Cycle Frame	IO-3,3	PU 8k2 3,3V	-
66	USB2	USB Data+ , Port2	IO-3,3	-	int. PD 15k in ICH4
67	GND	Ground	PWR	-	-
68	GND	Ground	PWR	-	-
69	AD16	PCI Address & Data Bus line	IO-3,3	-	-
70	CBE2#	PCI Bus Command and Byte enables 2	IO-3,3	-	-
71	AD17	PCI Address & Data Bus line	IO-3,3	-	-
72	USB3	USB Data+ , Port3	IO-3,3	-	int. PD 15k in ICH4
73	AD19	PCI Address & Data Bus line	IO-3,3	-	-
74	AD18	PCI Address & Data Bus line	IO-3,3	-	-
75	AD20	PCI Address & Data Bus line	IO-3,3	-	-
76	USB0#	USB Data- , Port0	IO-3,3	-	int. PD 15k in ICH4
77	AD22	PCI Address & Data Bus line	IO-3,3	-	-
78	AD21	PCI Address & Data Bus line	IO-3,3	-	-
79	AD23	PCI Address & Data Bus line	IO-3,3	-	-
80	USB1#	USB Data- , Port1	IO-3,3	-	int. PD 15k in ICH4
81	AD24	PCI Address & Data Bus line	IO-3,3	-	-
82	CBE3#	PCI Command and Byte enables 3	IO-3,3	-	-
83	VCC	Power +5V	PWR	-	-
84	VCC	Power +5V	PWR	-	-
85	AD25	PCI Address & Data Bus line	IO-3,3	-	-
86	AD26	PCI Address & Data Bus line	IO-3,3	-	-
87	AD28	PCI Address & Data Bus line	IO-3,3	-	-
88	USB0	USB Data+ , Port0	IO-3,3	-	int. PD 15k in ICH4
89	AD27	PCI Address & Data Bus line	IO-3,3	-	-
90	AD29	PCI Address & Data Bus line	IO-3,3	-	-
91	AD30	PCI Address & Data Bus line	IO-3,3	-	-
92	USB1	USB Data+ , Port1	IO-3,3	-	int. PD 15k in ICH4
93	PCIRST#	PCI Bus Reset	O-3,3	-	-
94	AD31	PCI Address & Data Bus line	IO-3,3	-	-
95	INTC#	PCI BUS Interrupt Request C	I-3,3	PU 8k2 3,3V	-
96	INTD#	PCI BUS Interrupt Request D	I-3,3	PU 8k2 3,3V	-
97	INTA#	PCI BUS Interrupt Request A	I-3,3	PU 8k2 3,3V	-
98	INTB#	PCI BUS Interrupt Request B	I-3,3	PU 8k2 3,3V	-
99	GND	Ground	PWR	-	-
100	GND	Ground	PWR	-	-

Note: The termination resistors in the table are already mounted on the ETX®-board. Refer to the design guide for information about additional termination resistors.

16.4 Connector X2 (ISA Bus)

Pin	Signal	Pin	Signal		Pin	Signal	Pin	Signal
1	GND	2	GND		51	VCC *	52	VCC *
3	SD14	4	SD15		53	SA6	54	IRQ5
5	SD13	6	MASTER#		55	SA7	56	IRQ6
7	SD12	8	DREQ7		57	SA8	58	IRQ7
9	SD11	10	DACK7#		59	SA9	60	SYSCLK
11	SD10	12	DREQ6		61	SA10	62	REFSH#
13	SD9	14	DACK6#		63	SA11	64	DREQ1
15	SD8	16	DREQ5		65	SA12	66	DACK1#
17	MEMW#	18	DACK5#		67	GND	68	GND
19	MEMR#	20	DREQ0		69	SA13	70	DREQ3
21	LA17	22	DACK0#		71	SA14	72	DACK3#
23	LA18	24	IRQ14		73	SA15	74	IOR#
25	LA19	26	IRQ15		75	SA16	76	IOW#
27	LA20	28	IRQ12		77	SA18	78	SA17
29	LA21	30	IRQ11		79	SA19	80	SMEMR#
31	LA22	32	IRQ10		81	IOCHRDY	82	AEN
33	LA23	34	IO16#		83	VCC *	84	VCC *
35	GND	36	GND		85	SD0	86	SMEMW#
37	SBHE#	38	M16#		87	SD2	88	SD1
39	SA0	40	OSC		89	SD3	90	NOWS#
41	SA1	42	BALE		91	DREQ2	92	SD4
43	SA2	44	TC		93	SD5	94	IRQ9
45	SA3	46	DACK2#		95	SD6	96	SD7
47	SA4	48	IRQ3		97	IOCHK#	98	RSTDRV
49	SA5	50	IRQ4		99	GND	100	GND

Notes: *To protect external power lines of peripheral devices, make sure that:
the wires have the right diameter to withstand the maximum available current
the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950.

16.4.1 Connector X2 (Signal Levels)

Pin 1–50: ISA Bus

Pin	Signal	Description	Type	Termination	Comment
1	GND	Ground	PWR	-	-
2	GND	Ground	PWR	-	-
3	SD14	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
4	SD15	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
5	SD13	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
6	MASTER#	ISA 16-Bit Master	I-5	PU 330R 5V	int. PU 50k 5V in
7	SD12	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
8	DREQ7	ISA DMA Request 7	I-5	PD 10k	int. PD 50k in PCI/ISA-B
9	SD11	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
10	DACK7#	ISA DMA Acknowledge 7	IO-5	-	int. PU 50k 5V in
11	SD10	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
12	DREQ6	ISA DMA Request 6	I-5	PD 10k	int. PD 50k in PCI/ISA-B
13	SD9	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
14	DACK6#	ISA DMA Acknowledge 6	IO-5	-	int. PU 50k 5V in
15	SD8	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
16	DREQ5	ISA DMA Request 5	I-5	PD 10k	int. PD 50k in PCI/ISA-B
17	MEMW#	ISA Memory Write	IO-5	PU 4k7 5V	int. PU 50k 5V in
18	DACK5#	ISA DMA Acknowledge 5	IO-5	-	int. PU 50k 5V in
19	MEMR#	ISA Memory Read	IO-5	PU 4k7 5V	int. PU 50k 5V in
20	DREQ0	ISA DMA Request 0	I-5	PD 10k	int. PD 50k in PCI/ISA-B
21	LA17	ISA Address Bus (SA17)	O-5	-	-
22	DACK0#	ISA DMA Acknowledge 0	IO-5	-	int. PU 50k 5V in
23	LA18	ISA Address Bus (SA18)	O-5	-	-
24	IRQ14	ISA Interrupt Request 14 / ROM Chip Select	IO-5	-	int. PU 50k 5V in
25	LA19	ISA Address Bus (SA19)	O-5	-	-
26	IRQ15	ISA Interrupt Request 15	I-5	-	int. PU 50k 5V in
27	LA20	ISA Latchable Address Bus	O-5	-	-
28	IRQ12	ISA Interrupt Request 12	I-5	-	int. PU 50k 5V in
29	LA21	ISA Latchable Address Bus	O-5	-	-
30	IRQ11	ISA Interrupt Request 11	I-5	-	int. PU 50k 5V in
31	LA22	ISA Latchable Address Bus	O-5	-	-
32	IRQ10	ISA Interrupt Request 10	I-5	-	int. PU 50k 5V in
33	LA23	ISA Latchable Address Bus	O-5	-	-
34	IO16#	ISA 16-Bit I/O Access	I-5	PU 330R 5V	int. PU 50k 5V in
35	GND	Ground	PWR	-	-
36	GND	Ground	PWR	-	-
37	SBHE#	ISA System Byte High Enable	IO-5	-	int. PU 50k 5V in
38	M16#	ISA 16-Bit Memory Access	IO-5	PU 330R 5V	int. PU 50k 5V in
39	SA0	ISA Address Bus	O-5	-	-
40	OSC	ISA Oscillator (CLK_ISA14#)	O-3,3	-	-
41	SA1	ISA Address Bus	O-5	-	-
42	BALE	ISA Buffer Address Latch Enable	IO-5	-	Bootstrap PD 4k7
43	SA2	ISA Address Bus	O-5	-	-
44	TC	ISA Terminal Count	IO-5	-	Bootstrap PD 4k7
45	SA3	ISA Address Bus	O-5	-	-
46	DACK2#	ISA DMA Acknowledge 2	IO-5	-	int. PU 50k 5V in
47	SA4	ISA Address Bus	O-5	-	-
48	IRQ3	ISA Interrupt Request 3	I-5	-	int. PU 50k 5V in
49	SA5	ISA Address Bus	O-5	-	-
50	IRQ4	ISA Interrupt Request 4	I-5	-	int. PU 50k 5V in

Note: The termination resistors in this table are already mounted on the ETX®-board. Refer to the design guide for information about additional termination resistors.

Pin 51–100: ISA BUS

Pin	Signal	Description	Type	Termination	Comment
51	VCC	Power +5V	PWR	-	-
52	VCC	Power +5V	PWR	-	-
53	SA6	ISA Address Bus	O-5	-	-
54	IRQ5	ISA Interrupt Request 5	I-5	-	int. PU 50k 5V in
55	SA7	ISA Address Bus	O-5	-	-
56	IRQ6	ISA Interrupt Request 6	I-5	-	int. PU 50k 5V in
57	SA8	ISA Address Bus	O-5	-	-
58	IRQ7	ISA Interrupt Request 7	I-5	-	int. PU 50k 5V in
59	SA9	ISA Address Bus	O-5	-	-
60	SYSCLK	ISA Bus Clock (CLK_SYS_ISA)	O-3,3	-	-
61	SA10	ISA Address Bus	O-5	-	-
62	REFSH#	ISA System Refresh Control	IO-5	PU 1k 5V	int. PU 50k 5V in
63	SA11	ISA Address Bus	O-5	-	-
64	DREQ1	ISA DMA Request 1	I-5	PD 10k	int. PD 50k in
65	SA12	ISA Address Bus	O-5	-	-
66	DACK1#	ISA DMA Acknowledge 1	IO-5	-	int. PU 50k 5V in
67	GND	Ground	PWR	-	-
68	GND	Ground	PWR	-	-
69	SA13	ISA Address Bus	O-5	-	-
70	DREQ3	ISA DMA Request 3	I-5	PD 10k	int. PD 50k in
71	SA14	ISA Address Bus	O-5	-	-
72	DACK3#	ISA DMA Acknowledge 3	IO-5	-	int. PU 50k 5V in
73	SA15	ISA Address Bus	O-5	-	-
74	IOR#	ISA I/O Read	IO-5	PU 4k7 5V	int. PU 50k 5V in
75	SA16	ISA Address Bus	O-5	-	-
76	IOW#	ISA I/O Write	IO-5	PU 4k7 5V	int. PU 50k 5V in
77	SA18	ISA Address Bus	O-5	-	-
78	SA17	ISA Address Bus	O-5	-	-
79	SA19	ISA Address Bus	O-5	-	-
80	SMEMR#	ISA System Memory Read	IO-5	PU 4k7 5V	int. PU 50k 5V in
81	IOCHRDY	ISA I/O Channel Ready	IO-5	PU 1k 5V	int. PU 50k 5V in
82	AEN	ISA Address Enable	IO-5	-	Bootstrap PD 4k7
83	VCC	Power +5V	PWR	-	-
84	VCC	Power +5V	PWR	-	-
85	SD0	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
86	SMEMW#	ISA System Memory Write	IO-5	PU 4k7 5V	int. PU 50k 5V in
87	SD2	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
88	SD1	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
89	SD3	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
90	NOWS#	ISA No Wait Staits	I-5	PU 330R 5V	int. PU 50k 5V in
91	DREQ2	ISA DMA Request 2	I-5	PD 10k	int. PD 50k in
92	SD4	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
93	SD5	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
94	IRQ9	ISA Interrupt Request 9	I-5	-	int. PU 50k 5V in
95	SD6	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
96	SD7	ISA Data Bus	IO-5	PU 10k 5V	int. PU 50k 5V in
97	IOCHK#	ISA I/O Channel Check	I-5	PU 4k7 5V	int. PU 50k 5V in
98	RSTDRV	ISA Reset	O-5	-	-
99	GND	Ground	PWR	-	-
100	GND	Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETX®-board. Refer to the design guide for information about additional termination resistors.

16.5 Connector X3 (VGA, LCD, Video, COM1 and COM2, LPT/Floppy, Mouse, Keyboard)

16.5.1 Flat-Panel Interfaces

ETX®-P3T modules can implement the following flat-panel interfaces:

- A LVDS flat-panel interface called JUMPtec Intelligent LVDS Interface (JILI)

LVDS Interface Pinout (JILI)

Pin	Signal	Pin	Signal
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSX	8	DDCK
9	DETECT#**	10	DDDA
11	LCDD016	12	LCDD018
13	LCDD017	14	LCDD019
15	GND	16	GND
17	LCDD013	18	LCDD015
19	LCDD012	20	LCDD014
21	GND	22	GND
23	LCDD08	24	LCDD011
25	LCDD09	26	LCDD010
27	GND	28	GND
29	LCDD04	30	LCDD07
31	LCDD05	32	LCDD06
33	GND	34	GND
35	LCDD01	36	LCDD03
37	LCDD00	38	LCDD02
39	VCC *	40	VCC *
41	JILI_DAT	42	LTGIO0**
43	JILI_CLK	44	BLON#
45	BIASON**	46	DIGON
47	COMP**	48	Y**
49	SYNC**	50	C**

Notes: *To protect external power lines of peripheral devices, make sure that:
the wires have the right diameter to withstand the maximum available current
the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950.
**This signal is not supported on the ETX®-P3T.

16.5.2 Parallel Port / Floppy Interfaces

You can configure ETX® parallel port interfaces as conventional PC parallel ports or as an interface for a floppy-disk drive. You can select the operating mode in the BIOS settings or by a hardware mode-select pin.

If Pin X3-51 (LPT/FLPY#) is grounded at boot time, the floppy support mode is selected. If the pin is left floating or is held high, parallel-port mode is selected. The mode selection is determined at boot time. It cannot be changed until the next boot cycle.

Parallel Port Mode Pinout

Pin	Signal	Pin	Signal
51	LPT/FLPY#	52	RESERVED
53	VCC *	54	GND
55	STB#	56	AFD#
57	RESERVED	58	PD7
59	IRRX	60	ERR#
61	IRTX	62	PD6
63	RXD2	64	INIT#
65	GND	66	GND
67	RTS2#	68	PD5
69	DTR2#	70	SLIN#
71	DCD2#	72	PD4
73	DSR2#	74	PD3
75	CTS2#	76	PD2
77	TXD2	78	PD1
79	RI2#	80	PD0
81	VCC *	82	VCC*
83	RXD1	84	ACK#
85	RTS1#	86	BUSY#
87	DTR1#	88	PE
89	DCD1#	90	SLCT#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

Floppy Port Mode Pinout

Pin	Signal	Pin	Signal
51	LPT/FLPY#	52	RESERVED
53	VCC *	54	GND
55	RESERVED	56	DENSEL
57	RESERVED	58	RESERVED
59	IRRX	60	HDSEL#
61	IRTX	62	RESERVED
63	RXD2	64	DIR#
65	GND	66	GND
67	RTS2#	68	RESERVED
69	DTR2#	70	STEP#
71	DCD2#	72	DSKCHG#
73	DSR2#	74	RDATA#
75	CTS2#	76	WP#
77	TXD2	78	TRK0#
79	RI2#	80	INDEX#
81	VCC *	82	VCC *
83	RXD1	84	DRV
85	RTS1#	86	MOT
87	DTR1#	88	WDATA#
89	DCD1#	90	WGATE#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

Notes: *To protect external power lines of peripheral devices, make sure that:
the wires have the right diameter to withstand the maximum available current
the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950

16.5.3 Connector X3 (Signal Levels)

Pin 1–50: **VGA**|**JILI**|**VIDEO**

Pin	Signal	Description	Type	Termination	Comment
1	GND	Ground	PWR	-	-
2	GND	Ground	PWR	-	-
3	R	Analog Video Out RGB - Red Channel	O	-	-
4	B	Analog Video Out RGB - Blue Channel	O	-	-
5	HSY	Horizontal Synchronization Pulse	O-5	PU 2k2 5V	-
6	G	Analog Video Out RGB - Green Channel	O	-	-
7	VSX	Vertical Synchronization Pulse	O-5	PU 2k2 5V	-
8	DDCK	Display Data Channel Clock	IO-5	PU 2k2 5V	-
9	DETECT#	Panel Hot-Plug Detection	nc	-	not supported
10	DDDA	Display Data Channel Data	IO-5	PU 2k2 5V	-
11	LCDDO16	LVDS Channel Data	O	-	-
12	LCDDO18	LVDS Channel Data	O	-	-
13	LCDDO17	LVDS Channel Data	O	-	-
14	LCDDO19	LVDS Channel Data	O	-	-
15	GND	Ground	PWR	-	-
16	GND	Ground	PWR	-	-
17	LCDDO13	LVDS Channel Data	O	-	-
18	LCDDO15	LVDS Channel Data	O	-	-
19	LCDDO12	LVDS Channel Data	O	-	-
20	LCDDO14	LVDS Channel Data	O	-	-
21	GND	Ground	PWR	-	-
22	GND	Ground	PWR	-	-
23	LCDDO8	LVDS Channel Data	O	-	-
24	LCDDO11	LVDS Channel Data	O	-	-
25	LCDDO9	LVDS Channel Data	O	-	-
26	LCDDO10	LVDS Channel Data	O	-	-
27	GND	Ground	PWR	-	-
28	GND	Ground	PWR	-	-
29	LCDDO4	LVDS Channel Data	O	-	-
30	LCDDO7	LVDS Channel Data	O	-	-
31	LCDDO5	LVDS Channel Data	O	-	-
32	LCDDO6	LVDS Channel Data	O	-	-
33	GND	Ground	PWR	-	-
34	GND	Ground	PWR	-	-
35	LCDDO1	LVDS Channel Data	O	-	-
36	LCDDO3	LVDS Channel Data	O	-	-
37	LCDDO0	LVDS Channel Data	O	-	-
38	LCDDO2	LVDS Channel Data	O	-	-
39	VCC	Power +5V	PWR	-	-
40	VCC	Power +5V	PWR	-	-
41	JILI_DAT	JILI I ² C Data Signal	IO-3,3	PU 4k7 3,3V	-
42	nc	-	nc	-	-
43	JILI_CLK	JILI I ² C Clock Signal	IO-3,3	PU 4k7 3,3V	-
44	BLON#	Display Backlight On	O-5	-	-
45	nc	-	nc	-	-
46	DIGON	Display Power On	O-5	-	-
47	nc	-	nc	-	-
48	nc	-	nc	-	-
49	nc	-	nc	-	-
50	Nc	-	nc	-	-

Note: The termination resistors in this table are already mounted on the ETX®-board. Refer to the design guide for information about additional termination resistors.

Pin 51–100: COM | LPT | Floppy | KB/MS/IR

Pin	Signal	Description	Type	Termination	Comment
51	LPT FLPY#	LPT / Floppy Interface Configuration Input	I-5	PU 4k7 5V	High: LPT, Low:
52	nc	-	nc	-	-
53	VCC	Power +5V	PWR	-	-
54	GND	Ground	PWR	-	-
55	STB# nc	LPT Strobe Signal	O-5	-	-
56	AFD# DENSEL	LPT Automatic Feed / Floppy Density Select	O-5	-	-
57	nc	-	nc	-	-
58	PD7 nc	LPT Data Bus D7	IO-5	-	-
59	IRRX	Infrared Receive	I-5	-	-
60	ERR# HDSEL#	LPT Error / Floppy Head Select	IO-5	-	-
61	IRTX	Infrared Transmit	O-5	-	-
62	PD6 nc	LPT Data Bus D6	IO-5	-	-
63	RXD2	Data Receive COM2	I-5	PU 100k 5V	-
64	INIT# DIR#	LPT Initiate / Floppy Direction	O-5	-	-
65	GND	Ground	PWR	-	-
66	GND	Ground	PWR	-	-
67	RTS2#	Request to Send COM2	O-5	PU 100k 5V	-
68	PD5 nc	LPT Data Bus D5	IO-5	-	-
69	DTR2#	Data Terminal Ready COM2	O-5	PU 100k 5V	-
70	SLIN# STEP#	LPT Select / Floppy Motor Step	O-5	-	-
71	DCD2#	Data Carrier Detect COM2	I-5	PU 100k 5V	-
72	PD4 DSKCHG#	LPT Data Bus D4 / Floppy Disk Change	IO-5	-	-
73	DSR2#	Data Set Ready COM2	I-5	PU 100k 5V	-
74	PD3 RDATA#	LPT Data Bus D3 / Floppy Raw Data Read	IO-5	-	-
75	CTS2#	Clear to Send COM2	I-5	PU 100k 5V	-
76	PD2 WP#	LPT Data Bus D / Floppy Write Protect Signal	IO-5	-	-
77	TXD2	Data Transmit COM2	O-5	-	Bootstrap PU 4k7
78	PD1 TRK0#	LPT Data Bus D1 / Floppy Track Signal	IO-5	-	-
79	RI2#	Ring Indicator COM2	I-5	PU 100k 5V	-
80	PD0 INDEX#	LPT Data Bus D0 / Floppy Index Signal	IO-5	-	-
81	VCC	Power +5V	PWR	-	-
82	VCC	Power +5V	PWR	-	-
83	RXD1	Data Receive COM1	O-5	PU 100k 5V	-
84	ACK# DRV	LPT Acknowledge / Floppy Drive Select	IO-5	-	-
85	RTS1#	Request to Send COM1	O-5	PU 100k 5V	Bootstrap PU 4k7
86	BUSY# MOT	LPT Busy / Floppy Motor Select	IO-5	-	-
87	DTR1#	Data Terminal Ready COM1	O-5	PU 100k 5V	Bootstrap PU 4k7
88	PE WDATA#	LPT Paper Empty / Floppy Raw Write Data	IO-5	-	-
89	DCD1#	Data Carrier Detect COM1	I-5	PU 100k 5V	-
90	SLCT# WGATE#	LPT Power On / Floppy Write Enable	IO-5	-	-
91	DSR1#	Data Set Ready COM1	I-5	PU 100k 5V	-
92	MSCLK	Mouse Clock	O-5	PU 4k7 5V	-
93	CTS1#	Clear to Send COM1	I-5	PU 100k 5V	-
94	MSDAT	Mouse Data	IO-5	PU 4k7 5V	-
95	TXD1	Data Transmit COM1	O-5	PU 100k 5V	Bootstrap PU 4k7
96	KBCLK	Keyboard Clock	O-5	PU 4k7 5V	-
97	RI1#	Ring Indicator COM1	I-5	PU 100k 5V	-
98	KBDAT	Keyboard Data	IO-5	PU 4k7 5V	-
99	GND	Ground	PWR	-	-
100	GND	Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETX®-board. Refer to the design guide for information about additional termination resistors.

16.6 Connector X4 (IDE 1, IDE 2, Ethernet, Miscellaneous)

Pin	Signal	Pin	Signal		Pin	Signal	Pin	Signal
1	GND	2	GND		51	SIDE_IOW#	52	PIDE_IOR#
3	5V_SB	4	PWGIN		53	SIDE_DRQ	54	PIDE_IOW#
5	PS_ON	6	SPEAKER		55	SIDE_D15	56	PIDE_DRQ
7	PWRBTN#	8	BATT		57	SIDE_D0	58	PIDE_D15
9	KBINH	10	LILED		59	SIDE_D14	60	PIDE_D0
11	RSMRST#	12	ACTLED		61	SIDE_D1	62	PIDE_D14
13	ROMKBCS#**	14	SPEEDLED		63	SIDE_D13	64	PIDE_D1
15	EXT_PRG**	16	I2CLK		65	GND	66	GND
17	VCC*	18	VCC*		67	SIDE_D2	68	PIDE_D13
19	OVCR#	20	GPCS#**		69	SIDE_D12	70	PIDE_D2
21	EXTSMI#	22	I2DAT		71	SIDE_D3	72	PIDE_D12
23	SMBCLK	24	SMBDATA		73	SIDE_D11	74	PIDE_D3
25	SIDE_CS3#	26	RESERVED		75	SIDE_D4	76	PIDE_D11
27	SIDE_CS1#	28	DASP_S**		77	SIDE_D10	78	PIDE_D4
29	SIDE_A2	30	PIDE_CS3#		79	SIDE_D5	80	PIDE_D10
31	SIDE_A0	32	PIDE_CS1#		81	VCC	82	VCC
33	GND	34	GND		83	SIDE_D9	84	PIDE_D5
35	PDIAG_S**	36	PIDE_A2		85	SIDE_D6	86	PIDE_D9
37	SIDE_A1	38	PIDE_A0		87	SIDE_D8	88	PIDE_D6
39	SIDE_INTRQ	40	PIDE_A1		89	RESERVED	90	RESERVED
41	RESERVED	42	RESERVED		91	RXD#	92	PIDE_D8
43	SIDE_AK#	44	PIDE_INTRQ		93	RXD	94	SIDE_D7
45	SIDE_RDY	46	PIDE_AK#		95	TXD#	96	PIDE_D7
47	SIDE_IOR#	48	PIDE_RDY		97	TXD	98	HDRST#
49	VCC*	50	VCC*		99	GND	100	GND

Notes: *To protect external power lines of peripheral devices, make sure that:
the wires have the right diameter to withstand the maximum available current
the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950
**This signal is not supported on the ETX®-P3T

16.6.1 Connector X4 (Signal Levels)

Pin 1–50: **IDE1** | **IDE2** | **ETHERNET** | **POWER/PM** | **MISC**

Pin	Signal	Description	Type	Termination	Comment
1	GND	Ground	PWR	-	-
2	GND	Ground	PWR	-	-
3	5V_SB	Supply of internal suspend Circuit	I	-	-
4	PWGIN	Power Good / Reset Input	I	-	-
5	PS_ON	Power Supply On	O-5	PU 10k 5V	-
6	SPEAKER	Speaker Output	O-5	-	int. PD 20k in ICH4
7	PWRBTN#	Power Button	I-5	-	-
8	BATT	Battery Supply	I	-	-
9	KBINH	Keyboard Inhibit Control Input	I-5	-	-
10	LILED	Ethernet Link LED	O-3,3	-	-
11	WDTRIG	Watschdog Trigger Input	I-3,3	PU 100k 3,3V	-
12	ACTLED	Ethernet Activity LED	O-3,3	-	-
13	nc	-	nc	-	-
14	SPEEDLED	Ethernet Speed LED	O-3,3	-	on at 100Mb/s
15	nc	-	nc	-	-
16	I2CLK	I ² C Bus Clock	O-5	PU 2k2 5V	-
17	VCC	Power +5V	PWR	-	-
18	VCC	Power +5V	PWR	-	-
19	OVCR#	Over Current Detect for USB	I-3,3	PU 10k 3,3V	-
20	nc	-	nc	-	-
21	EXTSMI#	System Management Interrupt Input	I-3,3	PU 10k 3,3V	-
22	I2DAT	I ² C Bus Data	IO-5	PU 2k2 5V	-
23	SMBCLK	SM Bus Clock	O-3,3	PU 2k2 3,3V	-
24	SMBDATA	SM Bus Data	IO-3,3	PU 2k2 3,3V	-
25	SIDE_CS3#	Secondary IDE Chip Select Channel 1	O-3,3	-	-
26	SMBALERT	-	IO-3,3	PU 10k 3,3V	Reserved
27	SIDE_CS1#	Secondary IDE Chip Select Channel 0	O-3,3	-	-
28	DASP_S	-	nc	-	not supported
29	SIDE_A2	Secondary IDE Adress Bus	O-3,3	-	-
30	PIDE_CS3#	Primary IDE Chip Select Channel 1	O-3,3	-	-
31	SIDE_A0	Secondary IDE Adress Bus	O-3,3	-	-
32	PIDE_CS1#	Primary IDE Chip Select Channel 0	O-3,3	-	-
33	GND	Ground	PWR	-	-
34	GND	Ground	PWR	-	-
35	PDIAG_S	80-conductor IDE cable Channel 1	I-3,3	PD 10k	not supported
36	PIDE_A2	Primary IDE Adress Bus	O-3,3	-	-
37	SIDE_A1	Secondary IDE Adress Bus	O-3,3	-	-
38	PIDE_A0	Primary IDE Adress Bus	O-3,3	-	-
39	SIDE_INTRQ	Secondary IDE Interrupt Request	I-3,3	PU 8k2 3,3V	-
40	PIDE_A1	Primary IDE Adress Bus	O-3,3	-	-
41	PM_BATLOW#	-	I-3,3	PU 10k 3,3V	Reserved
42	GPE1#	-	O	PU 8k2 3,3V	Reserved
43	SIDE_AK#	Secondary IDE DMA Acknowledge	O-3,3	-	-
44	PIDE_INTRQ	Primary IDE Interrupt Reqeuest	I-3,3	PU 8k2 3,3V	-
45	SIDE_RDY	Secondary IDE Ready	I-3,3	PU 4k7 3,3V	-
46	PIDE_AK#	Primary IDE DMA Acknowledge	O-3,3	-	-
47	SIDE_IOR#	Secondary IDE IO Read	O-3,3	-	-
48	PIDE_RDY	Primary IDE Ready	I-3,3	PU 4k7 3,3V	-
49	VCC	Power +5V	PWR	-	-
50	VCC	Power +5V	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETX®-board. Refer to the design guide for information about additional termination resistors.

Pin 51–100: IDE1 | IDE2 | ETHERNET | POWER/PM | MISC

Pin	Signal	Description	Type	Termination	Comment
51	SIDE_IOW#	Secondary IDE IO Write	O-3,3	-	-
52	PIDE_IOR#	Primary IDE IO Read	O-3,3	-	-
53	SIDE_DRQ	Secondary IDE DMA Request	I-3,3	-	-
54	PIDE_IOW#	Primary IDE IO Write	O-3,3	-	-
55	SIDE_D15	Secondary IDE Data Bus	IO	-	-
56	PIDE_DRQ	Primary IDE DMA Request	I-3,3	-	-
57	SIDE_D0	Secondary IDE Data Bus	IO	-	-
58	PIDE_D15	Primary IDE Data Bus	IO	-	-
59	SIDE_D14	Secondary IDE Data Bus	IO	-	-
60	PIDE_D0	Primary IDE Data Bus	IO	-	-
61	SIDE_D1	Secondary IDE Data Bus	IO	-	-
62	PIDE_D14	Primary IDE Data Bus	IO	-	-
63	SIDE_D13	Secondary IDE Data Bus	IO	-	-
64	PIDE_D1	Primary IDE Data Bus	IO	-	-
65	GND	Ground	PWR	-	-
66	GND	Ground	PWR	-	-
67	SIDE_D2	Secondary IDE Data Bus	IO	-	-
68	PIDE_D13	Primary IDE Data Bus	IO	-	-
69	SIDE_D12	Secondary IDE Data Bus	IO	-	-
70	PIDE_D2	Primary IDE Data Bus	IO	-	-
71	SIDE_D3	Secondary IDE Data Bus	IO	-	-
72	PIDE_D12	Primary IDE Data Bus	IO	-	-
73	SIDE_D11	Secondary IDE Data Bus	IO	-	-
74	PIDE_D3	Primary IDE Data Bus	IO	-	-
75	SIDE_D4	Secondary IDE Data Bus	IO	-	-
76	PIDE_D11	Primary IDE Data Bus	IO	-	-
77	SIDE_D10	Secondary IDE Data Bus	IO	-	-
78	PIDE_D4	Primary IDE Data Bus	IO	-	-
79	SIDE_D5	Secondary IDE Data Bus	IO	-	-
80	PIDE_D10	Primary IDE Data Bus	IO	-	-
81	VCC	Power +5V	PWR	-	-
82	VCC	Power +5V	PWR	-	-
83	SIDE_D9	Secondary IDE Data Bus	IO	-	-
84	PIDE_D5	Primary IDE Data Bus	IO	-	-
85	SIDE_D6	Secondary IDE Data Bus	IO	-	-
86	PIDE_D9	Primary IDE Data Bus	IO	-	-
87	SIDE_D8	Secondary IDE Data Bus	IO	-	-
88	PIDE_D6	Primary IDE Data Bus	IO	-	-
89	PM_RI#	-	I-3,3	PU 10k 3,3V	Reserved
90	PATADET	80-conductor IDE cable Channel 0	I-3,3	PD 10k	Reserved
91	RXD#	Ethernet Receive Differential Signal (RXD-)	I	-	121R between
92	PIDE_D8	Primary IDE Data Bus	IO	-	-
93	RXD	Ethernet Receive Differential Signal (RXD+)	I	-	121R between
94	SIDE_D7	Secondary IDE Data Bus	IO	-	int. PD 11k5 in ICH4
95	TXD#	Ethernet Transmit Differential Signal (TXD-)	O	-	100R between
96	PIDE_D7	Primary IDE Data Bus	IO	-	int. PD 11k5 in ICH4
97	TXD	Ethernet Transmit Differential Signal (TXD+)	O	-	100R between
98	HDRST#	Hard Drive Reset	O-3,3	-	-
99	GND	Ground	PWR	-	-
100	GND	Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETX®-board. Refer to the design guide for information about additional termination resistors.

17 Appendix F: JIDA Standard

Every board with an on-board BIOS extension supports the following function calls, which supply information about the board. Jumptec Intelligent Device Architecture (JIDA) functions are called via Interrupt 15h. Functions include:

- AH=Eah
- AL=function number
- DX=4648h (security word)
- CL=board number (starting with 1)

The interrupt returns a CL≠0 if a board with the number specified in CL does not exist. CL will equal 0 if the board number exists. In this case, the content of DX determines if the operation was successful. DX=6B6Fh indicates success; other values indicate an error.

17.1 JIDA Information

To obtain information about boards that follow the JIDA standard, use the following procedure.

- Call Get BIOS ID with CL=1.
The name of the first device installed will be returned.
If you see the result **Board exists** (CL=0), increment CL, and call **Get BIOS ID** again.
- Repeat until you see **Board not present** (CL≠0).
You now know the names of all boards within your system that follow the JIDA standard.
- You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

Note: Association between board and board number may change because of configuration changes. Do not rely on any association between board and board number. Always use the procedure described above to determine the association between board and board number.

Refer to the JIDA manual in the jidai1xx.zip folder, which is available from the Kontron Embedded Modules Web site, for further information on implementing and using JIDA calls with C sample code.

18 Appendix G: PC Architecture Information

The following sources of information can help you better understand PC architecture.

18.1 Buses

18.1.1 ISA, Standard PS/2 – Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

18.1.2 PCI/104

- Embedded PC 104 Consortium
The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI SIG
The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- PCI & PCI-X Hardware and Software Architecture & Design, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- PCI System Architecture, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

18.2 General PC Architecture

- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- Interfacing to the IBM Personal Computer, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3

- The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

18.3 Ports

18.3.1 RS-232 Serial

- EIA-232-E standard
The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.
- RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- National Semiconductor
The Interface Data Book includes application notes. Type "232" as search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor's Web site.

18.3.2 Serial ATA

- Serial AT Attachment (ATA) Working Group
This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web.
We recommend you also search the Web for information on 4.2 I/O cable, if you use hard disks in a DMA3 or PIO4 mode.

18.3.3 USB

- USB Specification
USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

18.4 Programming

- C Programmer's Guide to Serial Communications, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- Programmer's Guide to the EGA, VGA, and Super VGA Cards, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4

- The Programmer's PC Sourcebook, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas, Frank van GILLUWE, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8.

19 APPENDIX H: DOCUMENT-REVISION HISTORY

Revision	Date	Edited by	Changes
0.1	03.09.04	GDA	Created preliminary manual.
0.2	28.10.04	GDA	Added Serial IRQ information section 6.4.
0.3	03.11.04	GDA	Removed all references to digital LCD interface. Digital LCD interface is not supported.
1.0	17.01.05	GDA	Official release. Added power consumption values for 400MHz and 1.0GHz versions. Added CMOS battery consumption values in section 3.3.4. Removed Graphic Aperture node from section 15.4.1. Changed the default setting of USB EHCI Host Controller to Disabled in section 15.4.6. In section 15.6.1 changed the Active Trip Point and Passive Trip Point values to 40C-100C. Changed Critical Trip Point value to 40C-110C.
1.1	24.02.05	GDA	Added section 13.4 "ETX®-P3T onboard Fan connector".
1.2	07.06.05 13.07.05 09.09.05 30.09.05	GUL HRU HRU GUL	Updated I2C- and SM-Bus addresses Added power consumption values for 733MHz version Added note for Ethernet limitation Updated JIDA-Bus-numbers for I2C-bus; deleted clock throttling Added Signal Levels, Released for WEB
1.3	30.11.2005 01.12.2005 19.12.2005	AAY GUL GUL	Bios Setup Guide updated Updated pictures in chapter 13.4.3 Released for WEB
1.4	10.01.06 12.01.06 10.04.06 11.04.06 18.04.06	GUL GUL GUL GUL GUL	Changed contact address of Kontron America Added voltage range for CMOS Battery Corrected address of JILI-I2C-Bus Changed to new Kontron style Added supply current 5V_SB Added MTBF Updated 16.1 Connector Locations Updated Pin 35 + 90 at X4 (80-conductor ide cable detection) Corrected internal links in document Released for Web
1.5	17.05.06 16.05.07 18.05.07	GUL GUL GUL GUL	Changed Note about Ethernet limitation Updated to new Kontron Style Added Note "For UDMA-100/66 operation" Corrected max. UDMA-suppor